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Bezeichnung der Erfindung: High-speed electronic circuit having a cascode configuration
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : H03K 19/92

ENTSCHEIDUNG / DECISION

vom / of / du 10 October 1990

Anmelder / Applicant / Demandeur : Fujitsu Limited

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE PCT Article 17(3)(a) and Rule 40

Schlagwort / Keyword / Mot clé : "Lack of unity "a posteriori" (yes)"

Leitsatz / Headnote / Sommaire

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Case Number : W 5/89 - 3.5.1
International Application No. PCT/JP88/00758

D E C I S I O N
of the Technical Board of Appeal
of 10 October 1990

Applicant : Fujitsu Limited
1015, Kamikodanaka, Nakahara-ku
Kawasaki-shi, Kanagawa 211, JAPAN
(JP)

Representative : Hoffmann, Eitle & Partner
Postfach 81 04 20
D-8000 München 81
(DE)

Subject of the Decision : Protest according to Rule 40.2(c) of the Patent Cooperation Treaty made by the applicants against the invitation (payment of additional fees) of the European Patent Office (branch at The Hague) dated 26 October 1988.

Composition of the Board :

Chairman : P.K.J. van den Berg
Member : A.S. Clelland
Member : C. Holtz

Summary of Facts and Submissions

I. International patent application PCT/JP88/00758 was filed at the Japanese Patent Office on 28 July 1988.

II. On 26 October 1988 the European Patent Office, as competent International Search Authority (ISA), issued an invitation pursuant to Article 17(3)(a) and Rule 40.1 PCT to pay four additional search fees.

The ISA considered that the application did not comply with the requirement of unity of invention as set forth in Rule 13 PCT. This was said to be because the general problem underlying the invention was not novel and a solution to it had already been found or did not involve an inventive step having regard to the state of the art as illustrated by US-A-3 200 343 (D1). The claims were accordingly considered to require regrouping under the following distinct inventive concepts:

(1)	Claims 1-11	High speed electronic circuit having a cascode configuration and interface using the same
(2)	Claims 1, 12-21	Level shift circuit using high speed cascode circuitry
(3)	Claims 1, 22-25	Signal distribution circuit using high-speed cascode circuitry
(4)	Claims 1, 26	Signal synthesization circuit using high-speed cascode circuitry
(5)	Claims 27-50	Frequency band control amplification circuit using a cascode circuit

III. The applicant paid all the additional fees in due time and in a letter dated 6 December 1988 stated that the payment was made under protest. A statement of protest was enclosed, arguing that the disclosure of D1 did not cause the claims of the application to lack novelty or inventive step.

Reasons for the Decision

1. Pursuant to Rule 40.2(c) PCT and Article 154(3) EPC the Boards of Appeal of the EPO are responsible for deciding on a protest made by an applicant against additional search fees charged under Article 17(3)(a) PCT by the EPO when acting as the ISA.

2. The protest complies with the formal requirements of Rules 40.2 and 40.3 PCT and is accordingly admissible.

3. The objection of lack of unity made by the ISA only arose after a preliminary search had been carried out and was accordingly made "a posteriori", i.e. after taking prior art into consideration. The question of whether the EPO when acting as an ISA is entitled to raise an "a posteriori" lack of unity objection or whether such an objection pre-empts the separate preliminary examination under Chapter II PCT was referred to the Enlarged Board of Appeal of the EPO. In its recent decision G 1/89 of 2 May 1990, to be published, the Enlarged Board concluded that "a posteriori" objection of lack of unity was allowable since the ISA only formed a provisional opinion on novelty and inventive step for the purpose of carrying out an effective search which did not constitute a substantive examination in the normal sense of that term. The Enlarged Board added that consideration of the

requirement of unity of invention should always be made with a view to giving the applicant fair treatment and that the charging of additional fees under Article 17(3)(a) PCT should be made only in clear cases; restraint should be exercised in the assessment of novelty and inventive step and borderline cases preferably resolved in favour of the applicant.

4. The claims of the application can be grouped as follows:

(1) The "high speed electronic circuit" of Claims 1 to 5 and "interface circuit" of Claims 6 to 11 (Figs. 8 to 10)

(2) The "level shift circuit" of Claims 12 to 15 and "interface circuit" of Claim 16(Figs. 14 to 18); the "signal discrimination circuit" of Claims 17 to 21 (Figs. 19 to 27);

(3) The "signal distribution circuit" of Claims 22 to 25 (Figs. 28 to 37);

(4) The "signal synthesization circuit" of Claim 26 (Figs. 38 to 41);

(5) The "frequency band control amplification circuit" of Claims 27 to 50 (Figs. 45 to 68).

All the claims of claim groups (1) to (4) are dependent on Claim 1, whereas Claim 27, the first claim of claim group (5), is independent. The remaining claims of this group are dependent on Claim 27.

5. As claimed in Claim 1 the invention is directed to a "high speed electronic circuit" comprising in essence the following features:

(1) a "current drive circuit" including an input transistor the emitter of which is "operatively grounded" and the base of which receives an input signal;

(2) a load transistor circuit, the emitter of the load transistor being connected to a collector of the input transistor and its base being "operatively grounded";

(3) a bias current source connected to the emitter (of the load transistor) to maintain a base-emitter voltage (at the same level) whether the transistor is "turned off" or turned on".

The expression "operatively grounded" refers to grounding of the signal path as opposed to d.c. grounding. The claim defines a cascode configuration although this is not stated explicitly. The expression "turned on" is not considered to imply saturation.

6. The application includes a second independent claim, Claim 27, which is directed to a "frequency band control amplification circuit" and includes in somewhat different language the features (1) and (2) of Claim 1 but does not include feature (3); instead, the claim is in essence limited by the following feature:

(4) frequency band control means "operatively connected" to the common point of the two transistors, for controlling a capacitance between the emitter of the load transistor and ground and thereby controlling the frequency band of an output signal.

7. In the protest (page 2, lines 5 to 18) the applicant implicitly accepts that features (1) and (2) of Claims 1 and 27 are known from D1; this can indeed be seen to be the case from a consideration of the figure of D1. These are the only features common to Claims 1 and 27 and no single general inventive concept can be identified linking the group (5) claims with the claims of the remaining groups all of which are, as noted at point 4 above, dependent on Claim 1. Claim 27 and those claims dependent on it therefore lack unity with Claim 1 and the remaining groups of claims.

8. Turning now to Claim 1, in the protest the applicant also accepts that "the construction of the bias current source of the present invention, per se, is similar to the circuit of the document". It is then however stated that in contrast to the citation, the bias current source of the invention provides a constant current corresponding to the base-emitter current of the load transistor and serving to cancel the effect of this current and thereby eliminate the effect of stray capacitance.

This is not reflected in the actual wording of Claim 1, which does not require a constant current source. Feature (3) of the claim is somewhat unclear but apparently requires that the bias current source maintain the load transistor base-emitter voltage at the same level whether the transistor is conducting or not. In D1 the current through a load resistor 18 of the input transistor 10 "is maintained at approximately a fixed level" (column 5, lines 56 to 69), so that the voltage at point 31 is maintained constant (column 4, lines 62 to 67), implying that the base-emitter voltage of transistor 11 is also maintained constant.

Even if the reference to a bias current source were taken as implying a constant bias current source, then on the interpretation of the expression "constant current" which is supported by the description the claim still lacks novelty. This is because the expression "constant bias current source" apparently covers the arrangement of a resistor and a voltage source as shown in the embodiments of Figs. 10a, 10b, 32, 33, 36, 41 and 43 of the application; this arrangement is disclosed in D1. For the input transistor of D1 the combination of resistor 14 and battery 15 are referred to at column 3, lines 21, 22 as a "constant current source", so that by analogy the same must be true of resistor 18 and battery 19 connected to the emitter of the load transistor. The above-quoted passage of D1 stating that the current through a load resistor 18 of the input transistor 10 "is maintained at approximately a fixed level" (column 5, lines 56 to 69) also suggests this.

The subject-matter of Claim 1, no matter how the reference to the "bias current source" is interpreted, accordingly lacks novelty. Therefore, contrary to the Appellant's statement in the last paragraph of page 2 of his protest, the use of the said cascode configuration can no longer be considered as an inventive concept common to all the inventions claimed.

9. Thus, no general inventive concept is claimed which links the claims of groups (1) to (4). However, this does not automatically lead to the conclusion that these remaining groups of claims therefore lack unity of invention. Rule 13.1 PCT merely requires that a group of inventions be linked by a single general inventive concept; it does not specify that this concept be explicitly claimed. It is therefore necessary to consider whether any further general inventive concept links some or all of groups (1) to (4).

The Appellant has suggested that even if his main argument is not accepted the claims should be regrouped into three groups rather than five, consisting of groups (1), (3) and (4), group (2) and group (5).

With regard to the first of these new groups a common inventive concept is alleged to reside in how an adverse effect of a stray capacitance on a line between an input circuit and an output circuit should be eliminated. In the interface circuit (group 1) the relationship of the input circuit and the output circuit is said to have a 1:1 correspondence, in the signal distribution circuit (group 3) a 1:N correspondence and in the signal synthesisation circuit (group 4) an N:1 correspondence.

In the view of the Board it is obvious to the skilled person that reduction of the effect of such stray capacitances is inherent to the use of the said known cascode configuration and that consequently such reduction cannot be maintained as constituting an inventive concept linking the inventions of groups (1), (3) and (4).

No other combination of features which could form a general inventive concept linking some or all of the groups has been put forward by the Appellant or can be identified by the Board. Accordingly the Board can only conclude that the invitation by the International Search Authority to pay additional fees was fully justified.

Order

For these reasons, it is decided that:

Refund of any of the additional search fees is refused.

The Registrar: The Chairman:

M. Kiehl P.K.J. van den Berg