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**D E C I S I O N**  
**of 4 April 2003**

**Case Number:** T 1104/99 - 3.4.3

**Application Number:** 93901921.2

**Publication Number:** 0617840

**IPC:** H01L 21/76

**Language of the proceedings:** EN

**Title of invention:**

Negative biasing of isolation trench fill to attract mobile positive ions away from bipolar device regions

**Applicant:**

HARRIS CORPORATION

**Opponent:**

-

**Headword:**

Mobile ions/HARRIS

**Relevant legal provisions:**

EPC Art. 56

Guidelines C-III, 4.9

**Keyword:**

"Technical functional feature in a method claim"

"Inventive step (yes) - after amendment"

**Decisions cited:**

G 0002/88, G 0006/88, T 0231/85, T 0848/93

**Catchword:**

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Boards of Appeal

Chambres de recours

**Case Number:** T 1104/99 - 3.4.3

**D E C I S I O N**  
**of the Technical Board of Appeal 3.4.3**  
**of 4 April 2003**

**Appellant:** HARRIS CORPORATION  
1025 West NASA Boulevard  
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**Representative:** Meddle, Alan Leonard  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 13 August 1999  
refusing European patent application  
No. 93 901 921.2 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** G. L. Eliasson  
M. J. Vogel

## Summary of Facts and Submissions

I. European patent application No. 93 901 921.2 was refused in a decision of the examining division dated 13 August 1999. The ground for the refusal was that the application did not meet the requirement of inventive step having regard to the prior art documents

D1: US-A-4 470 062;

D2: Patent abstracts of Japan, vol. 13, No. 038 (E-709) & JP-A-63-236 343 together with its English translation; and

D3: US-A-4 037 306.

II. Claim 1 according to the main request forming the basis of the decision under appeal reads as follows:

"1. A method of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device (11) comprising the steps of:

- (a) providing a semiconductor integrated circuit structure having an insulating support substrate (15), a semiconductor layer (21) of a first conductivity type having a top surface (22), a bottom surface overlaying said support substrate, and side surfaces (27), said semiconductor layer containing a semiconductor device (11) having at least one PN junction, said semiconductor device including a semiconductor region (35) of a second conductivity type, opposite to said first conductivity type and forming a first PN junction of said at least one PN junction with said semiconductor layer (21), wherein

no PN junction, including said first PN junction, intersects a side surface of said semiconductor layer, and wherein said semiconductor device (11) is coupled to receive a plurality of bias voltages; a trench extending from the top surface of the semiconductor layer (21) to the substrate surface and surrounding said semiconductor device (11) and having sidewalls which define said side surfaces of said semiconductor layer; dielectric material (29) disposed along said sidewalls and also on a bottom portion of said trench; and material (31) capable of distributing a voltage therethrough formed in said trench (23), so as to be insulated from said semiconductor layer (21) by dielectric material (29) disposed along said sidewalls of said trench and being insulated from said substrate by dielectric material (29) disposed along said bottom portion of said trench, said material capable of distributing a voltage therethrough being confined to said trench (23), so that said material (31) capable of distributing a voltage therethrough does not extend over said top surface of said semiconductor layer (21) and overlies any PN junction, including said first PN junction; and

- (b) applying a prescribed bias voltage to the material (31) in said trench (23) capable of distributing a voltage and establishing the magnitude of said prescribed bias voltage at a voltage which is relatively negative when compared with a most positive one and a most negative one of said plurality of bias voltages to electrically prevent mobile

positive ions from being transported into said semiconductor region (35) in response to temperature bias stress and thereby affecting an operational parameter of said semiconductor device."

III. The reasoning of the examining division in the decision under appeal, as far as being relevant to the present case, can be summarized as follows:

- (a) Document D3 which is considered the closest prior art discloses a method comprising the steps of providing a semiconductor integrated circuit structure having, among others, an isolation trench extending from a top surface of a semiconductor substrate and surrounding a semiconductor device. The trench is lined with a dielectric material and filled with a material capable of distributing a voltage therethrough.
- (b) The claimed method differs from that disclosed in document D3 in that (i) the substrate is an insulating support substrate whereas document D3 discloses a silicon substrate; (ii) a prescribed bias voltage is applied to the material filling the trenches which is relatively negative as compared with a most positive one and a most negative one of the bias voltages applied to the device surrounded by the trench, whereas in document D3, no specific bias voltages are mentioned; and (iii) the claimed method relates to the prevention of mobile ions from reaching the semiconductor device, whereas document D3 does not mention mobile ions at all. The latter difference (iii) relates to a result to be achieved by means of the method, and is therefore not considered to be technical features of the claimed method.

- (c) The replacement of a semiconductor substrate by an insulating substrate is considered to be an obvious use of a well-known equivalent (feature (i)).

Regarding feature (ii), it is taught in document D3 that the conductive material filling the trenches may be used to form an interconnect system for the semiconductor device. Document D1, which discloses a semiconductor device surrounded with a trench filled with conductive material, teaches that it is advantageous to connect the trench to ground potential in order to provide shielding, where the ground may be the lowest potential of the device.

Therefore, the skilled person following the teaching of documents D3 and D1 would arrive at *all of the technical features* of claim 1 according to the main request without requiring an inventive step.

- (d) The application in suit is silent on the origin of the mobile ions, so that it is not possible to identify any possible differences between the application and the cited prior art in this respect. It is however known from document D2 that mobile ions may be present in the molding resin of semiconductor devices. Given that the skilled person would carry out the modifications (i) and (ii) of the method of document D3 without employing inventive skills, it must be concluded that the effect of preventing mobile ions from migrating into the device regions would also occur when combining the teaching of documents D3 and D1.

IV. The appellant (applicant) lodged an appeal on 12 October 1999, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 9 December 1999.

V. In response to a communication and a telephone consultation with the Board, the appellant filed new application documents with the letters dated 7 October 2002 and 25 October 2002.

The appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of one of the following requests:

**Main request**

Claims: 1 to 4 according to the main request filed with the letter dated 7 October 2002;

Description: pages 1, 1a, and 3 filed with the letter dated 25 October 2002,  
pages 2 and 4 to 6 as originally filed;

Drawings: Sheet 1/1 as originally filed;

**Auxiliary request**

Claims: 1 to 4 according to the auxiliary request filed with the letter dated 7 October 2002;

Description and Drawings as for the main request.

Oral proceedings are requested in case the Board does not intend to grant any of the above requests.

VI. Claim 1 according to the main request presently under consideration differs from that considered in the decision under appeal in that the step (b) in the former claim reads as follows:

"(b) applying a prescribed bias voltage to the material (31) in said trench (23) capable of distributing a voltage and establishing the magnitude of said prescribed bias voltage at a voltage which is no more positive than the mean value of a most positive one and a most negative one of said plurality of bias voltages to electrically prevent mobile positive ions from being transported into said semiconductor region (35) in response to temperature bias stress and thereby affecting an operational parameter of said semiconductor device."

Claims 2 to 4 are dependent claims.

VII. The appellant presented essentially the following arguments in support of his requests:

(a) Document D3 uses isolating trenches which may be used as circuit interconnect to provide conductors to the semiconductor devices, but does not disclose what type of potential may be applied to the conductors in the trenches. Document D1 discloses the use of isolating trenches which are connected by a top layer extending over the device regions where a ground potential is applied to the top layer to perform a shielding function. Thus, none of the documents D3 and D1 discloses the problem of mobile positive ions. Moreover, documents D1 and D3 relate to different problems,



so that the skilled person would not have any reason to combine documents D1 and D3, let alone for the purpose of preventing mobile positive ions from reaching the semiconductor device regions.

- (b) Document D2 discloses the problem of mobile ions only in the context of a so-called "walled-emitter" bipolar transistor where the emitter/base/collector pn-junctions intersect an isolation trench surrounding the semiconductor layer in which the transistor is formed. Mobile ions at the isolation trench may cause a parasitic NMOS transistor along the isolation trench to turn on. In order to assure that the parasitic NMOS transistor is turned off, it is taught in document D2 to fill the isolation trench with polysilicon which acts as a gate of the parasitic NMOS transistor, and to apply an appropriate voltage to the "gate".
  
- (c) Since no pn-junction intersects the isolation trench in the device of document D3, a parasitic MOS transistor cannot arise from the presence of mobile ions at the isolation trench. Thus, skilled person would have no reason to employ the teaching of document D2 to the device of document D3.

### **Reasons for the Decision**

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and Clarity - Main Request*

Claim 1 according to the main request is based on claim 8 as filed and the features disclosed on page 1, first paragraph, page 2, last paragraph to page 3, first paragraph, and Figure 1 of the application as filed. Claims 2 and 3 are based on claims 10 and 11 as filed, and claim 4 is based on page 4, first paragraph of the application as filed. The claims are furthermore clear.

For the above reasons, the Board finds that the requirements of Articles 123(2) and 84 EPC are met.

3. *Inventive step - Main Request*

3.1 Document D3, which was considered closest prior art in the decision under appeal, discloses a bipolar integrated circuit on silicon substrate 54 with V-shaped isolation trenches 68, 70, 72 (cf. abstract; Figure 5). The walls of the V-shaped isolation trenches are lined with an insulating material 98, 100, 102 and the interior of the isolation trenches are filled with metal 112, 114, 116 in order to obtain a planar structure (cf. column 2, lines 36 to 38; column 5, lines 4 to 34; Figures 8 to 10). The metal 112, 114, 116 in the isolation trenches may be used as wiring layer which is connected to the wiring layer 130 formed above the semiconductor device (cf. Figure 12; column 5, lines 49 to 53; column 6, lines 11 to 20).

Document D3 does not mention the detrimental effect of mobile ions on the device performance and also therefore, in contrast to the method of claim 1 according to the main request, does not disclose a method of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device.

3.2 Document D1 discloses a bipolar integrated circuit on a conventional silicon substrate (cf. abstract). The devices are separated from each other with isolation trenches 19 which are lined with oxide 18a (cf. Figures 3a, 3b; column 2, line 60 to column 3, line 8). The interior of the trenches 19 are filled with doped polysilicon 20 (cf. Figure 3c; column 3, lines 9 to 16). In order to prevent "charge leakage from the electrodes etc.", the polysilicon regions 20 in the trenches may be grounded (cf. Figure 3e; column 3, lines 36 to 49).

Document D1 does not discuss the problem of mobile ions entering the device regions, and therefore does not disclose a method of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device.

3.3 Document D2 discloses a bipolar transistor which is surrounded by an isolation trench 151, 152 (cf. abstract). The walls of the isolation trench are lined with an insulating film 16, and the interior of the isolation trench is filled with a conductive material 17. The transistor of document D2 is a so-called "walled-emitter" transistor where the pn-junctions between the collector 14, base 24 and emitter 26 of the bipolar transistor are intersecting the isolation trench. This construction has the problem that mobile ions at the isolation trench may cause a parasitic NMOS transistor consisting of the emitter, base, and collector at the isolation trench to turn on, thereby turning the bipolar transistor on. In order to ensure that the parasitic NMOS transistor is kept turned-off, it is suggested in document D2 to fill the interior of the isolation trench with conductive material 17 which functions as a "gate" of the parasitic NMOS transistor, and to apply an appropriate voltage to the "gate". The conductive material 17 in

the isolation trenches is connected to a bias potential which is the ground potential or a negative potential which is the lowest potential in the device (cf. translation, paragraph bridging pages 5 and 6).

- 3.3.1 The method of claim 1 according to the main request differs from that of document D2 in that (i) the substrate is an isolating substrate, whereas in document D2, it is a semiconductor substrate; and (ii) no pn-junction of the semiconductor device intersects a side surface of the semiconductor layer in which the semiconductor device is formed, whereas in the device of document D2, the base/emitter and base/collector pn-junction are intersecting the side surface of the semiconductor layer in which the transistor is formed.
- 3.4 In the decision under appeal, it was acknowledged that documents D1 and D3 did not disclose the problem of mobile ions in a semiconductor device, and that a method resulting from a combination of these documents would not, strictly speaking, be "a method of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device". Nevertheless, the examining division held that this difference was not a technical feature but merely a result to be achieved by means of the method (cf. item III(b) above). Furthermore, since the method obtained by combining the teaching of documents D3 with that of document D1 evidently would have the effect of preventing positive ions from moving into the device regions, the examining division held that the method of documents D3 and D1 must therefore be considered as a "method of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device" (cf. item III(d) above).

- 3.4.1 The Board is however not able to follow the examining division's finding that the functional feature of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device is not a technical feature for the following reasons:

In the decisions G 2/88 and G 6/88 of the Enlarged Board (OJ EPO 1990, 93 and 114, respectively), the Enlarged Board held that a functional feature in a use claim should be construed as a functional technical feature (G 6/88, reasons 7.1). Although the above decisions of the Enlarged Board discuss "use" claims, it is also pointed out that use claims and method claims are both directed to an activity, and thus the reasoning given in the above decisions of the Enlarged Board is also applicable for other method claims (cf. G 6/88, reasons 2.2 to 2.5; T 848/93, reasons 3.3; as well as Guidelines C-III, 4.9). In the present case, it follows that the method of operating the device, in particular the step of applying a bias voltage, has to prevent mobile ions from reaching the device regions, and is thus a technical feature defining the scope of the claim.

In the Board's view, therefore, the skilled person had no incentive to combine the documents D3 and D1 with a view to provide a method of preventing mobile positive ions from moving into a semiconductor region of a semiconductor device.

- 3.5 In the light of the above considerations, the Board considers document D2 to be the closest prior art, since it deals with the detrimental effects of mobile ions in an integrated circuit device.

As the appellant convincingly argued, however, the device in the claimed method has all its pn-junctions spaced away from the isolation trenches, and therefore,

the problem addressed in document D2 - current flowing through a parasitic transistor due to the presence of mobile ions collecting *in the isolation trenches* - will not occur, since such a parasitic transistor structure of the type known from document D2 is not present in the device in the claimed method. Document D2 as well as all the other cited prior art documents are silent about other problems which may be caused by mobile ions. The skilled person would not therefore consider document D2 to be relevant when confronted with the problem of mobile ions in active regions of a semiconductor device having no pn-junctions intersecting a side surface, as defined in claim 1 (cf. the application in suit page 1, first two paragraphs).

Therefore, in the Board's judgement, the subject matter of claim 1 according to the main request involves an inventive step within the meaning of Article 56 EPC.

## **Order**

### **For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents according to the main request as specified under item V above.

The Registrar:

The Chairman:

M. Zawadzka

R. K. Shukla