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D E C I S I O N
of 28 February 2002

Case Number: T 0824/99 - 3.5.1
Application Number: 94301246.8
Publication Number: 0613287
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G06F 13/16

Language of the proceedings: EN

Title of invention:
Image communication method and apparatus

Applicant:
CANON KABUSHIKI KAISHA

Opponent:
-

Headword:
Image communication apparatus/CANON

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-



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Boards of Appeal

Chambres de recours

Case Number: T 0824/99 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 28 February 2002

Appellant:

CANON KABUSHIKI KAISHA
30-2, 3-chome, Shimomaruko
Ohta-ku
Tokyo (JP)

Representative:

Beresford, Keith Denis Lewis
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

Decision under appeal:

**Decision of the Examining Division of the
European Patent Office posted 9 February 1999
refusing European patent application
No. 94 301 246.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. V. Steinbrener
Members: R. S. Wibergh
S. C. Perryman

Summary of Facts and Submissions

I. This appeal is against the decision of the Examining Division to refuse European patent application No 94 301 246.8.

II. The Examining Division held that the subject-matter of claim 1 was obvious having regard to the following documents:

D1: EP-A-0 456 447

D2: SE-A-8 900 132 as reported in the Derwent abstract AN 90-318490.

III. A new set of claims 1 to 6 replacing all previous claims were filed with the grounds of appeal on 18 June 1999.

Claim 1 read as follows:

"An image communication apparatus comprising:

communication means (100) for performing the transmission or reception of data to or from an external communication apparatus via a communication line;

memory means (101) for storing received data and data to be transmitted;

recording means (106-108, 111-115) for recording data stored in said memory means;

a first bus (120) linking said communication means

to said memory;

a second bus (122) by means of which said recording means can fetch data from said memory means;

interface means (191) adapted to receive data from or transmit data to an external device; and

a third bus (121) connected to said interface means;

characterised in that said apparatus further comprises:

data bus selecting means (110) to which said first, second and third buses are connected in parallel, the data bus selecting means having a bus for linking a selected one of said first, second and third buses with said memory means; and

control means (109) for controlling the link performed by said data bus selecting means in accordance with the respective access requirements of said communication device, said recording means and said interface means".

Claim 5 was an independent claim directed to a "method for controlling an image communication apparatus".

IV. In a communication from the Board annexed to a summons to attend oral proceedings, the preliminary opinion was given that the invention lacked an inventive step over D2.

V. Oral proceedings before the Board were held on

28 February 2002. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the set of claims filed on 18 June 1999.

VI. At the end of the oral proceedings the Chairman announced the order of the Board's decision.

Reasons for the Decision

1. The invention according to claim 1 is an apparatus capable of sending and receiving faxes, printing data, and communicating - by means of an interface - with an external device such as a personal computer (PC). Each of the fax controller, the printer and the interface is connected to a separate data bus. A common data memory is linked to all three buses. "Data bus selecting means" with associated "control means" are provided to select which bus should be connected to the memory. Sharing the memory between the units permits the size and cost of the apparatus to be reduced.
2. D2 discloses a fax apparatus to which an external printer 12 and an external PC 14 are connected. Received fax data are stored in memory (either EPROM 6,7 or RAM 8) under the control of a first processor, CPU1. A second processor CPU2 controls the data transmission from this memory to the printer 12. This CPU is linked also to the PC via the interface 13. The aim in D2 is to allow received faxes to be printed out on a separate, high-quality printer.
3. The Board is of the opinion that D2 discloses the features of the preamble of claim 1. In particular, the

three buses set out in the claim are identified with the line connecting the memory with CPU1, the line connecting the memory with CPU2, and the line connecting the PC interface with CPU2. The depicted lines are taken to symbolise buses.

4. As to the characterising part of claim 1, the appellant has argued that D2 describes no data bus selecting means and control means in the meaning of the present application. According to the appellant, the tasks performed by these means are in D2 divided between the two CPUs, CPU1 controlling the selection of the first bus and CPU2 controlling the selection of the other two buses.
5. The Board however takes the view that the phrasing in claim 1 relating to the data bus selection means and the control means is so generalized that it covers also a configuration comprising two separate CPUs. Also the description contains hardly any information at all about these means. Figures 1 and 2 may suggest that the "data bus selector" 110 is a bus switch without processing capacity controlled by a "memory intervention circuit" having such capacity, but this cannot be regarded as more than a hint to the structure of the particular embodiment shown. The fact remains that the claim does not exclude selection and control means comprising two processors.
6. The Board has also considered the situation on the construction of the claim contended for by the appellant. The appellant argues that, although the data bus selecting means and the control means might conceivably be implemented by a microcomputer, they cannot be identified with the two separate CPUs shown

in D2, which constitute a more complex structure. Furthermore, it is a deliberate choice in D2 that one CPU handles the image data in fax format and the other the data in printer format. Therefore the skilled person would not consider altering this configuration.

7. This Board cannot accept this view. Generally, a computer-controlled system can be defined in terms of the tasks it has to perform. The designer must decide what kind of control is suitable, what processing power is needed, what kind of processor or processors are required, etc. It is not denied that such considerations may sometimes be of an inventive nature, for example if a particularly efficient configuration is proposed. In the present case, however, the particular design of the "data bus selecting means" and "control means" is not described as being essential for achieving any particular advantages. Hence, the objective technical problem solved might in fact only be seen in providing an alternative solution. Furthermore, as already noted, the claimed solution is hardly described at all. This implies that the skilled person was expected to be able to design the selection means practically without instructions, and consequently would simply rely on one of available design alternatives. Therefore it is not possible to conclude that the substitution of a single CPU (or microcomputer) for a pair of CPUs involved an inventive step.

8. It is furthermore noted that already D1 (Figure 4) describes a printer comprising a "data bus selector" 18 under the control of a read/write control circuit 21 serving to connect one of two data buses to a common RAM 11. This additional piece of prior art confirms the

view that the skilled person would have a number of design alternatives at hand, and in particular would recognise that the bus selection and control functions could be performed by separate circuits rather than by a CPU, as in D2. Moreover, the extension from a selection between two buses (D1) to a selection among three buses (the invention) is straightforward.

9. If the proposed circuit configuration was in any case obvious to the skilled person it is not significant that it might be less complex than D2, as submitted by the appellant. (Incidentally, it may not be self-evident that a system with one comparatively powerful CPU - in itself a complex component - is actually simpler than a system with two less advanced CPUs.) The circuit complexity is a factor which the skilled person would consider together with other relevant factors, such as overall performance and cost. For the same reason it appears irrelevant whether the use of two CPUs in D2 is intentional or not.

10. It is therefore concluded that even if the appellant's interpretation of claim 1 were accepted, the subject-matter of claim 1 does not involve an inventive step (Article 56 EPC). Independent method claim 5 is open to the same objections. The appellant's request for grant of a patent must therefore be refused.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

M. Kiehl

S. Steinbrener