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D E C I S I O N
of 16 May 2003

Case Number: T 0546/99 - 3.4.3

Application Number: 92304719.5

Publication Number: 0517408

IPC: H01L 21/82

Language of the proceedings: EN

Title of invention:
Sram cell and structure with polycrystalline p-channel load devices

Applicant:
STMicroelectronics, Inc.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 52(1), 54, 56
EPC R. 67

Keyword:
"Novlety (yes - after amendments)"
"Inventive step (yes - after amendments)"
"Reimbursement of appeal fee not substantiated"

Decisions cited:
-

Catchword:
-

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Case Number: T 0546/99 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 16 May 2003

Appellant: STMicroelectronics, Inc.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 17 December 1998 refusing European patent application No. 92 304 719.5 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
J. H. Van Moer

Summary of Facts and Submissions

I. European patent application No. 92 304 719.5 was refused by the decision of the Examining Division of 17 December 1998. The grounds for refusal were that the subject-matter of claim 1 was not inventive and that the subject-matter of claim 12 was not new having regard to the prior art document:

D3: EP-A-0 297 350.

II. The appellant (applicant) lodged an appeal on 17 February 1999, paying the appeal fee the same day. The statement setting out the grounds of appeal was filed on 27 April 1999.

III. With the Board's communication dated 25 October 2002 the appellant was informed that the request for refund of the appeal fee submitted with the statement of grounds of appeal had not been substantiated by the appellant. The Board, moreover, could not recognize any substantial procedural violation in the proceedings before the Examining Division.

Amendments to the claims and the description were subsequently filed by the appellant with the letters dated 24 December 2002 and 19 March 2003 in response to communications from the Board.

IV. The appellant requests that the decision under appeal be set aside, that the appeal fee be refunded in accordance with Rule 67 EPC and that a patent be granted on the basis of the following patent application documents:

Claims: 1 to 17, filed with the letter of 19 March 2003

Description: pages 1, 2 and 4 to 10, as originally filed
page 3, filed with the letter of 7 June 1995
page 3a and 3c, filed with the letter of 24 December 2002
pages 3b and 11, filed with the letter of 19 March 2003

Drawings: Sheets 1/4 to 4/4, filed with the letter of 20 July 1992

The wording of independent claims 1 and 11 is as follows:

"1. A method of producing a semiconductor device structure with polycrystalline p-channel load devices of an integrated circuit comprising the steps of:
providing a first n-channel field effect device (14);
providing a first insulating layer (34) disposed over the n-channel field effect device with an opening to expose an underlying conductive structure comprising at least a portion of a n-type source/drain region of said n-channel field effect device;
providing a contact layer (35;36) over the exposed underlying conductive structure defining a portion of a shared contact region, said contact layer making electrical contact with said source/drain region (22) of said n-channel field effect device;

providing a first p-type polysilicon layer (40,42) comprising a first gate electrode (42) of a first p-channel field effect device disposed over a portion of the first insulating layer (34);
providing a first gate oxide layer (44); and
providing a second polysilicon layer (46),
comprising the source/drain region and channel region of the first p-channel field effect device, disposed over the first gate electrode (42) of the first p-channel field effect device and the contact layer (35;36), said source/drain region of said p-channel device having p-type conductivity, characterised in that:
said first p-type polysilicon layer (40,42) also comprises a region (40) in contact with said contact layer (35;36), said gate oxide layer (44) being disposed over the first gate electrode (42) of the first p-channel field effect device and said region (40) of said first p-type polysilicon layer in contact with said contact layer (35;36); and in that
the source/drain region of the p-channel device makes electrical contact with the underlying conductive structure through said region (40) of said first p-type polysilicon layer and said contact layer (35;36) and
wherein said contact layer is formed from materials selected from the group comprising metal; metal silicide; n-type polysilicon overlaid with a metal silicide; and silicide overlaid with p-type polysilicon."

"11. A structure consisting of a portion of a semiconductor integrated circuit comprising:
a first n-channel field effect device (14);

a first insulating layer (34) disposed over the n-channel field effect device with an opening to expose an underlying conductive structure comprising at least a portion of the n-type source/drain region of said n-channel field effect device;
a contact layer (35;36) over the exposed underlying conductive structure defining a portion of a shared contact region, said contact layer making electrical contact with said source/drain region (22) of said n-channel field effect device;
a first p-type polysilicon layer (40;42) comprising a first gate electrode (42) of a first p-channel field effect device disposed over a portion of the first insulating layer (34);
a first gate oxide layer (44); and
a second polysilicon layer (46), comprising the source/drain region and channel region of the first p-channel field effect device, disposed over the first gate electrode (42) of the first p-channel field effect device and the contact layer (35; 36), said source/drain region of said p-channel device having p-type conductivity, characterised in that:
said first p-type polysilicon layer (40,42) also comprises a region (40) in contact with said contact layer (35;36), said gate oxide layer (44) being disposed over the first gate electrode (42) of the first p-channel field effect device and said region (40) of said first p-type polysilicon layer in contact with said contact layer (35;36); and in that
the source/drain region of the p-channel device makes electrical contact with the underlying conductive structure through said region (40) of

said first p-type polysilicon layer and said contact layer (35;36), and
wherein said contact layer is formed from material selected from the group comprising: metal; metal silicide; n-type polysilicon overlaid with a metal silicide; and silicide overlaid with p-type polysilicon."

V. In the decision under appeal the Examining Division argued that the method of producing a semiconductor device structure according to claim 1 differed from the method disclosed in document D3 only in that the contact region was formed by patterning and etching. No inventive step could, however, be recognized in these steps, since they would readily occur to the skilled person for forming this region.

Moreover, all the features of the semiconductor integrated circuit according to independent claim 12 were anticipated by the structure disclosed in document D3 (cf. Fig. 4).

VI. The appellant argued as follows in support of his request:

- The new independent method and device claims are based on former claim 12 but have been clarified and each one recast in the two-part form with the preamble based on document D3.

- The method according to claim 1 and the semiconductor structure according to claim 11 are new over the disclosure of document D3 (Fig. 3), since this document does not disclose that the n+ polysilicon layer 412 is in contact with the

silicide layer.

- Moreover, document D3 addresses a different problem from the one of the application, namely to minimize the space required for a static, random access memory (SRAM) cell by using "pull-down" n-channel trench transistors and a buried layer ground plate. It does not deal, however, with the problem of parasitic diode formation between the gates of the p-channel transistors and the source/drain regions of the n-channel transistors, since this problem is more acute in stacked devices if the option of independent optimization of the resistors is retained. To modify the semiconductor device disclosed in document D3 in order to use a p-doped polysilicon layer as the gate of the p-channel transistor, the upper part of the n+ polysilicon layer 412 would have to be doped with p-type impurities. This would, however, create a pn junction within this layer (cf. Fig. c attached to the statement of grounds). For these reasons, the required modifications to the prior art would have a detrimental effect on the operation of the device.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

In the decision under appeal, there were no objections raised against the claims under Article 123(2) EPC, and the Board is also satisfied that the claims as amended

during the examination proceedings complied with Article 123(2) EPC.

In the course of the appeal proceedings the independent device claim 11 has been amended to specify that the first polysilicon layer comprises a region 40 which is in contact with the contact layer 36, and that the gate oxide layer 44 is disposed over the gate electrode 42 of the first p-channel field effect device and over the region 40 of the first polysilicon layer in contact with the contact layer. These features are derived from the semiconductor device structure shown in the application (cf. Fig. 6 and column 5, lines 21 to 39 of the published application). Independent method claim 1 has been amended to follow the wording of independent device claim 11.

Moreover, to improve the clarity of the claims, layer 40, 42 has been identified as the first polysilicon layer and layer 46 as the second polysilicon layer.

Furthermore, the relevant parts of the description have been adapted to the claims.

The Board is, for these reasons, satisfied that the amendments made fulfill the requirement of Article 123(2) EPC.

3. *Novelty*

Document D3 discloses (cf. Figs. 2, 4 and 6) a semiconductor integrated device comprising in the wording of claim 11 the following features (the features of document D3 which correspond to the

elements of the claim have been added in parentheses):

a first n-channel field effect device (Fig. 4, the "n+S/D" region of transistors 210', 216' shown in Fig. 6);
a first insulating region disposed over the n-channel field effect device with an opening (Fig. 4, via 4/4) to expose an underlying conductive structure comprising at least a portion of the n-type source/drain region of said n-channel field effect device;
a contact layer (Fig. 4, "silicide") over the exposed underlying conductive structure defining a portion of a shared contact region, said contact layer making electrical contact with said source/drain region of said n-channel field effect device;
a first polysilicon layer (Fig. 4, n+ poly 2, indicated by numeral 412) comprising a first gate electrode of a first p-channel field effect device (Fig. 4, poly 3 indicated by numeral 410 and "p+ S/D") disposed over a portion of the first insulating layer;
a first gate oxide layer; and a second polysilicon layer (Fig. 4, poly 3 indicated by numeral 410), comprising the source/drain region and channel region of the first p-channel field effect device, disposed over the first gate electrode of the first p-channel field effect device and the contact layer, said source/drain region of said p-channel device having p-type conductivity.

Document D3 discloses, therefore, that the polysilicon layer 412 which corresponds to the first polysilicon layer 40, 42 is doped n^+-type while according to claim 11 it is doped p-type.

Furthermore, in the integrated circuit disclosed in

document D3 the polysilicon layer 412 and the silicide layer do not share a common contact region contrary to what is specified in the characterizing portion of claim 11 (the first p-type polysilicon layer 40, 42 comprises a region 40 in contact with the contact layer 35, 36).

For these reasons, the semiconductor structure according to claim 11 is new over the disclosure of document D3 in the sense of Article 54 EPC. As claim 1 is directed to a method of producing a semiconductor structure having all the features of claim 11, its subject-matter is new for the same reasons.

4. *Inventive step*

4.1 The problem addressed by the application in suit is to avoid the formation of parasitic pn-junctions in SRAM cells at the locations where the gate of a p-channel transistor contacts a source/drain region of a n-channel transistor (cf. column 1, line 50 to column 2, line 8 and Figs. 1 and 2).

4.2 The semiconductor device structure according to claim 11 comprises a first n-channel field effect device (FET) 14 having a gate oxide layer 16, a gate electrode 18 and source/drain regions 22 (cf. Fig. 6). A portion of the source/drain region 22 of this FET is in electrical contact with the metal containing contact layer 36. In order to save space, a p-channel FET is stacked above the n-channel FET and is separated from it by the insulating layer 34 (cf. column 4, lines 42 to 47). The gate electrode 40 as well as the source/drain and channel regions 46 of this p-channel FET are made of p-type polysilicon. The electrical

contact between the gate of the p-channel FET and the source/drain region 22 of the n-channel FET is made through the metal containing contact layer 36. The contact layer 40 is thus a shared contact between a n-channel and a p-channel FET used in a SRAM cell. The shared contact connects materials having different conductivity types and the use of a metal or a metal silicide interconnect layer prevents the formation of a pn-junction (cf. column 5, lines 35 to 46).

4.3 The primary object of document D3 is the provision of a SRAM cell of minimum size by making use of trench pull-down transistors and a buried-layer ground plate (cf. column 4, lines 1 to 4). The semiconductor structure disclosed in document D3 uses separate polysilicon regions as the gate and source/drain/channel regions of the p-channel load transistor (cf. Fig. 4, layer 410 poly 3 and layer 412 poly 2). A silicide layer is employed at the via opening to short out the pn junction formed between the p-type source/drain of the p-channel load transistor and the n-type source/drain of the n-channel transfer transistor (cf. column 6, lines 7 to 9).

4.6 The overall structure of the SRAM cell disclosed in this document is, however, completely different from the one claimed in claim 11 and is, therefore, not a state of the art from which the skilled person would start.

The Board concurs with the appellant in that it is not feasible to modify the semiconductor structure disclosed in document D3 in order to obtain a SRAM cell including p-channel FETs having p-type gates. To create a p-type gate the upper part of the n+ polysilicon

layer 412 would have to be doped with p-type impurities to change its conductivity type. This modification would, however, form parasitic diodes at the interfaces where the p-type and the n-type polysilicon meet and would have a detrimental effect on the operation of the device.

4.5 This reasoning applies not only to the semiconductor structure according to claim 11 but also to the method of claim 1, since the latter produces the semiconductor structure as defined in claim 11.

4.6 In the Board's judgement, therefore, the subject-matters of claims 1 and 11 involve an inventive step in the sense of Article 56 EPC and accordingly meet the requirements of Article 52(1) EPC.

5. *Reimbursement of the appeal fee*

The appellant requested with the statement of grounds of appeal that the appeal fee be refunded in accordance with Rule 67 EPC.

Rule 67 EPC, however, foresees the reimbursement of the appeal fee if the appeal is allowable and if such reimbursement is equitable by reason of a substantial procedural violation.

The appellant has not pointed out in his submissions any procedural violation that might have occurred during the proceedings before the Examining Division, and the Board also cannot recognize any procedural violation so that it would not be equitable to refund the appeal fee.

For these reasons, the request for reimbursement of the appeal fee is refused.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The request for reimbursement of the appeal fee is refused.

3. The case is remitted to the first instance with the order to grant a patent in the following version:

Claims: 1 to 17, filed with the letter of 19 March 2003

Description: pages 1, 2 and 4 to 10, as originally filed
page 3, filed with the letter of 7 June 1995
page 3a and 3c, filed with the letter of 24 December 2002
pages 3b and 11, filed with the letter of 19 March 2003

Drawings: Sheets 1/4 to 4/4, filed with the letter of 20 July 1992

The Registrar: The Chairman:

P. Martorana R. K. Shukla