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Boards of Appeal

Chambres de recours

Case Number: T 0523/99 - 3.4.3

**D E C I S I O N**  
of 9 October 2003 correcting errors in the decision  
of the Technical Board of Appeal 3.4.3  
of 27 September 2002

**Appellant:**

ZAIDAN HOJIN HANDOTAI KENKYU SHINKOKAI  
Kawauchi  
Aoba-ku  
Sendai-shi  
Miyagi-ken, 980 (JP)

**Representative:**

Sparing Röhl Henseler  
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Postfach 14 04 43  
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**Decision under appeal:**

Decision of the Examining Division of the  
European Patent Office posted 15 December 1998  
refusing European patent application  
No. 93 103 283.3 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** G. L. Eliasson  
M. J. Vogel

**It is decided that:**

Decision T 523/99 of 27 September 2002 shall be corrected pursuant to Rule 89 EPC in that the section "Drawings" in item V of the "Summary of Facts and Submissions" shall read:

**"Drawings:** Figures 1 to 20 filed with the letter dated 26 July 2002."

The Registrar:



U. Bultmann

The Chairman:



R. K. Shukla

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**D E C I S I O N**  
of

27 September 2002

**Case Number:** T 0523/99 - 3.4.3

**Application Number:** 93103283.3

**Publication Number:** 0559133

**IPC:** H01L 29/72

**Language of the proceedings:** EN

**Title of invention:**  
Static induction thyristor

**Applicant:**  
ZAIDAN HOJIN HANDOTAI KENKYU SHINKOKAI

**Opponent:**  
-

**Headword:**  
-

**Relevant legal provisions:**  
EPC Art. 56

**Keyword:**  
"Inventive step (yes - after amendments)"

**Decisions cited:**  
-

**Catchword:**  
-



Case Number: T 0523/99 - 3.4.3

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of the Technical Board of Appeal 3.4.3  
of

**Appellant:**

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## Summary of Facts and Submissions

I. European patent application No. 93 103 283.3 was refused in a decision of the examining division dated 15 December 1998. The ground for the refusal was that the subject matter of claims 1 to 13 filed with the letter dated 21 May 1997 did not involve an inventive step having regard to the prior art documents

D1: Patent Abstracts of Japan, vol. 16, No. 130, 2 April 1992 & JP-A-2-292 770 (24 December 1991); and

D2: S. M. Sze, "Physics of Semiconductor Devices", 2nd. Ed. (J. Wiley & Sons, New York, 1981), page 456.

II. The reasoning of the examining division in the decision under appeal can be summarized as follows:

(a) Document D1 is considered the closest prior art and discloses a Static Induction Thyristor (SIT) having a monolithically integrated p-channel Metal-Insulator-Semiconductor Field Effect Transistor (MISFET) for turning off the SIT.

The device of claim 1 differs from that of document D1 only in that a well of n-type conductivity is formed on a part of a surface of the channel of the SIT, and that the MISFET is formed in the well so that the drain is formed within the well and the channel is formed in the surface of the well, whereas in document D1, the MISFET is formed directly in the channel region of the SIT.

(b) The technical problem can thus be regarded as avoiding punch-through in a MISFET, a problem well-known in the art.

(c) A skilled person faced with the problem of avoiding punch-through in the MISFET of the device of document D1 would consider the teaching of document D2 which discloses a MISFET formed in a well region having a higher doping concentration than that of the substrate.

III. The appellant (applicant) lodged an appeal on 11 February 1999, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 23 April 1999 together with new application documents and the following document

D3: J. R. Hook and H. E. Hall, "Solid State Physics", 2nd Ed. (J. Wiley & Sons, Chichester, 1991), page 190.

IV. In a communication under Article 11(2) of the Rules of Procedure of the Boards of Appeal annexed to a summons to oral proceedings, the Board introduced further pages of the same text-book which furnished document D2:

D2a: S. M. Sze, "Physics of Semiconductor Devices", 2nd. Ed. (J. Wiley & Sons, New York, 1981), pages 456 to 488,

and informed the appellant of its provisional opinion that the application did not appear to meet the requirements of inventive step having regard to documents D1 and D2a.

V. In response to the communication of the Board and to a telephone consultation dated 5 August 2002, the appellant filed new claims and amended description pages with the letters dated 9 July 2002, 26 July 2002, and 6 August 2002.

The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

**Claims:** 1 to 13 filed with the letter dated 6 August 2002;

**Description:** pages 1 to 4, 8, 13 to 18, 23 to 38 filed with the letter dated 26 July 2002 (pages 9 to 12 and 19 to 22 deleted), pages 5, 5a, 6, 7 filed with the letter dated 6 August 2002;

**Drawings:** Figures 1 to 10 filed with the letter dated 26 July 2002.

Oral proceedings were requested in case the above request was not to be allowed.

VI. Claim 1 according to the above request reads as follows:

"1. A static induction device comprising:  
a static induction thyristor at least having a cathode region (23) of n type conductivity having high impurity concentration, an anode region (21) and a pair of gate regions (31) of p type conductivity having high impurity concentration, and a channel region (22) of n type conductivity having low impurity concentration, having a gate spacing of normally off type;

a p-channel MISFET at least having a channel region of n type conductivity, a gate insulating film (26, 261) formed on said channel region, a gate electrode (25) formed on said insulating film (26, 261), a drain region (32) of p type

conductivity, said drain region (32) being formed overlapping said cathode region (23),

a capacitor comprising the gate region (31), the gate insulating film (26, 261) formed on the gate region (31), and the gate electrode (25),

wherein said cathode (23) and drain region (32) are connected to each other through a cathode electrode (231),

wherein said static induction thyristor and said MISFET are merged onto a single monolithic chip, characterized in that

said MISFET is a depletion type p-channel MISFET having a well (59) of n type conductivity formed on a part of a surface of said channel region (22) of the static induction thyristor between said cathode region (23) and said gate region (31), said drain region (32) having high impurity concentration being formed within said well (59), said gate insulating film (26, 261) formed over said well (59), said well (59) having an impurity concentration higher than that of said channel region (22) of the static induction thyristor and a source region (312) of said depletion type p-channel MISFET having high impurity concentration formed within the well (59) and electrically connected to said gate region (31), the source and the drain regions (312, 32) being self-aligned with the gate electrode (25)."

Claims 2 to 13 are dependent claims.

VII. The appellant presented essentially the following arguments in support of his request:



- (a) The device known from document D1 suffers from the effects of a trade-off between the impurity concentration of the channel region of the SIT and the spacing between the gate regions. If the spacing between the gate regions is chosen to be small in order to allow high frequency operation, the MISFET formed in the channel region of the SIT will experience punch-through between the source and drain region. This punch-through causes a short circuit between the gate region and the cathode which turns off the SIT and prevents the SIT from being turned on.

Furthermore, the gate length of the MISFET fluctuates due to misalignments of the masks used to form the gate electrode and the drain region so that the on-voltage of the MISFET fluctuates thereby causing a fluctuation in turn-off characteristics from device to device.

- (b) The claimed device has the advantage over the prior art device of document D1 in that the MISFET is formed in a well region having a higher doping concentration than the channel region of the SIT. This allows for setting the source-drain distance to be small without having the risk of punch-through. Furthermore, the claimed device has also the advantage that the source and drain regions of the MISFET are self-aligned with the gate electrode, which means that the channel length between source and drain is entirely determined by the size of the gate electrode. This allows a precise control of the channel length which increases the yield.

Document D1 does not contain any hint with regard to the nature of fluctuation in the on-voltage of

the MISFET due to misalignment of photolithographic masks.

### Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and clarity*

Claim 1 is based on claim 1 as filed together with the feature disclosed on page 24, lines 5 to 11 of the application as filed, and has been amended for clarity. Claims 2 to 13 are based on the embodiments of Figures 6 to 9 and 11 to 22 of the application as filed (now Figures 1 to 16).

The Board is therefore satisfied that the requirements of Articles 84 and 123(2) EPC are met.

3. *Inventive step*

3.1 Document D1, which is considered the closest prior art, discloses a static induction thyristor (SIT) having a MISFET integrated on the same chip. The SIT comprises an n-type cathode region 23, an n-type channel region 22, a p-type anode region 21, and a pair of p-type gate regions 31 formed in the channel region 22 (cf. Figure 4(a) and (b)). The MISFET, which is a normally-on p-type MISFET, is formed in the n-type channel region 22 of the SIT and comprises a p-type drain region 32 and a gate electrode 25. The gate electrode is formed on a gate insulating film 26 and extends between the drain region and the gate region 31 of the SIT which also acts as the source region of the MISFET. A portion of the gate electrode 25 extends over the gate region 31 of the SIT and forms a

capacitor together with the gate region which is used to turn on the SIT. The drain region 32 is connected to the cathode region 23 through a cathode electrode 23'.

- 3.2 The device of claim 1 differs from that of document D1 in that (i) the p-channel MISFET is formed in an n-type well region which is formed on a part of a surface of the channel region of the static induction thyristor (SIT) and has a higher doping concentration than the channel region of the SIT; and (ii) the source and drain regions are formed self-aligned with the gate electrode.

In the device of document D1 on the other hand, the MISFET is formed directly in a surface region of the channel region of the static induction thyristor. Furthermore, the source and drain regions in the device of document D1 are not formed self-aligned with the gate electrode, since the gate electrode is patterned using photolithography after that the gate (source) region 31 is formed.

- 3.3 As described in the application in suit, the prior art device suffers from the problem that in order to avoid punch-through between source and drain of the MISFET, the source-drain distance has to be rather large which increases the on-resistance. If punch-through occurs, it is not possible to turn on the SIT. If on the other hand, the on-resistance of the MISFET is too high, it is not possible to turn off the SIT at high anode currents (cf. page 3, line 4 to page 4, line 5; page 4, line 18 to page 5, line 4).

Furthermore, the claimed device has the advantage that the source and drain regions of the MISFET are self-aligned with the gate electrode, which means that the channel length between source and drain is entirely determined by the size of the gate electrode. This

allows a precise control of the channel length which minimizes deviations in device characteristics, thereby improving the yield of manufacturing the device (cf. application as filed, page 24, lines 5 to 18).

3.4 The problem addressed by the application in suit is therefore to provide an electrostatic induction device comprising a normally off SIT and a normally on MISFET which is reliably operable when the gate length of the MISFET is chosen to be small and can produced with a high yield.

3.5 Document D2a discloses a MISFET structure presented under the acronym "HMOS" where a single ion-implantation (Figure 52a) or a double ion-implantation (Figure 52b) is carried out in order to increase the punch-through voltage (cf. page 488). As shown in Figures 52a and 52b, a well region is formed which has a higher doping concentration (here "p") than that of the substrate ("p<sup>-</sup>"). The well region is sufficiently deep and wide so that the source and drain regions are formed within the well region.

Document D2a does not, however, disclose that the source and drain regions are self-aligned with the gate electrode.

3.6 In the decision under appeal, the examining division held the provision of a higher doped well region for the p-channel MISFET to be obvious (cf. item II(c) above). The Board concurs with this view that a skilled person faced with the task of increasing the punch-through voltage of the p-channel MISFET of the device of document D1 would consider the teaching of document D2a where the channel and at least the drain region are formed within a higher doped well region.

- 3.7 With respect to the claims under consideration in the decision under appeal, claim 1 as amended further specifies that the source and drain regions of the MISFET are self-aligned with the gate electrode. As correctly pointed out by the appellant, the cited prior art documents D1 and D2a do not disclose this feature.
- 3.8 When the device of document D1 is modified such that the MISFET is formed in an n-type well having higher impurity concentration than that of the channel region, the channel length of the MISFET is shortened correspondingly. Although the shorter channel length has the desired property of lowering the on-resistance of the MISFET while keeping the punch-through voltage at a sufficiently high level, certain device characteristics, such as the on-voltage, show greater fluctuations due to misalignments of the photolithographic masks.
- 3.9 Although it is well-known *per se* to provide a MISFET with self-aligned source and drain regions, the self-alignment technique is usually employed in integrated circuits where the individual MISFETs have very small dimensions. For the power device disclosed in document D1, on the other hand, self-aligned source and drain regions are not necessary, since the distance between source and drain, i.e. the channel length of the MISFET, has to be kept relatively large in order to prevent punch-through in the very low doped channel region. Therefore, compared to the channel length of the MISFET, the fluctuations of the channel length due to misalignments of the photolithography mask used to pattern the gate electrode are small, and consequently, the deviations of device characteristics due to mask misalignment are not significant in the device of document D1.

Moreover, the construction disclosed in document D1 has the advantage that the gate electrode can be formed to overlap the gate region 31 of the SIT so that the capacitor, which is used for turning the SIT on, can easily be formed. Such a simple construction is not possible when source and drain are self-aligned with the gate electrode, since a portion of the gate electrode has to extend over the gate region of the SIT. Therefore, the skilled person would not find any incentive to self-align source and drain with the gate electrode in the device of document D1.

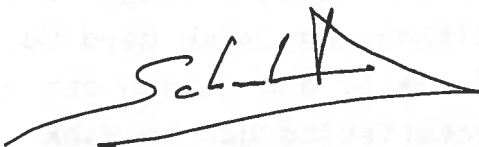
- 3.11 Therefore, in the Board's judgement, the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents according to the appellant's request as specified under item V above.

The Registrar:



R. Schumacher

The Chairman:



R. K. Shukla