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D E C I S I O N
of 12 March 2003

Case Number: T 0498/99 - 3.4.3

Application Number: 92104203.2

Publication Number: 0503605

IPC: H01L 29/72

Language of the proceedings: EN

Title of invention:

Insulated gate type bipolar-transistor with overvoltage protection

Applicant:

DENSO CORPORATION

Opponent:

-

Headword:

Insulated gate type bipolar-transistor with overvoltage protection/DENSO CORPORATION

Relevant legal provisions:

EPC Art. 52(1), 56

Keyword:

"Inventive step (yes - after amendments)"

Decisions cited:

-

Catchword:

-



Case Number: T 0498/99 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 12 March 2003

Appellant: DENSO CORPORATION
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Aichi-Pref. (JP)

Representative: Winter, Brandl, Fürniss, Hübner, Röss,
Kaiser, Polte
§ Partnerschaft
Patent- und Rechtsanwaltskanzlei
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 11 December 1998
refusing European patent application
No. 92 104 203.2 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
M. J. Vogel

Summary of Facts and Submissions

- I. In a decision dispatched on 11 December 1998, the examining division refused European application No. 92 104 203.2 on the ground that claim 1 was not new having regard to the disclosure in document

D2: IEEE Electron Device Letters, Vol. 10,
No. 129, December 1986, pp. 686-688 (Baglia)

interpreted in the light of the common general knowledge in the art as represented by document

D1: S. M. Sze, "Physics of Semiconductor Devices", 2nd edition, New York: Wiley & Sons, 1981, pp. 194 - 195.

With reference to the dependent claims, the examining division also cited the following document

D3: Patent Abstracts of Japan, Vol. 10, No. 129,
(E-403) [2186], May 14, 1986 & JP-A-60 260 152.

- II. A notice of appeal requesting that the decision under appeal be set aside was filed on 22 February 1999, and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 24 April 1999, together with a main request and one auxiliary request. The appellant requested that a patent be granted on the basis of the main request or the auxiliary request. Oral proceedings were requested should the Board intend to reach an adverse decision.

- III. In a communication accompanying the summons to oral proceedings, the Board expressed the preliminary view that claim 1 of the main request before it lacked novelty over document D2, and claim 1 of the auxiliary

request lacked an inventive step over the disclosure in document D2 in combination with document D3 or the following document which had been cited in the search report

D5: EP-A-0 080 044.

IV. Oral proceedings took place on 12 March 2003. At the oral proceedings, the appellant filed a new request replacing all previous requests. The request contains claims 1 to 7, with claims 2 to 7 being dependent on claim 1.

Claim 1 reads as follows:

"1. An insulated gate type bipolar-transistor comprising a first semiconductor layer (4) of a first conductivity type;
a second semiconductor layer (3) of a second conductivity type having an interface with said first semiconductor layer (4) and a main surface opposite said interface, a first pn junction being formed at said interface;
a third semiconductor layer (7) of said first conductivity type formed in said second semiconductor layer (3) adjoining said main surface and forming with said second semiconductor layer (3) a second pn junction terminating at said main surface;
a fourth semiconductor layer (8) of said second conductivity formed in said third semiconductor layer (7) adjoining said main surface and forming with said third semiconductor layer (7) a third pn junction terminating at said main surface;
a gate electrode (10) formed on a channel region adjacent to the surface of said third semiconductor layer (7) extending between said second semiconductor layer (3) and said fourth semiconductor layer (8) via a gate insulation layer (11);

a source electrode (9) directly contacting both of said third and fourth semiconductor layers (7 and 8);
a drain electrode (1) directly contacting said first semiconductor layer (4); wherein
said second semiconductor layer (3) has such an impurity concentration and such a thickness that a depletion region extending from said second junction between said third semiconductor layer (7) and said second semiconductor layer (3) toward the inside of said second semiconductor layer (3) reaches said first semiconductor layer (4) through said second semiconductor layer (3) at a voltage applied between said drain electrode (1) and said source electrode (9) lower than a drain-source voltage at which a critical electric field causing partial avalanche breakdown at or in the vicinity of said second semiconductor layer (3), and minority carriers for said semiconductor layer (3) are injected from said first semiconductor layer (4) to said second semiconductor layer (3), and flow to said source electrode (9);
characterized in that a fifth semiconductor layer (6) of said second conductivity type is disposed at or in the vicinity of the first pn junction between said first semiconductor layer (4) and said second semiconductor layer (3), said fifth semiconductor layer (6) having a higher impurity concentration than said second semiconductor layer (3) and having a pattern leaving a contact surface between said first and second semiconductor layers (4, 3) whereby carriers can be transferred there through."

V. The arguments presented by the appellant can be summarised as follows.

The invention relates to over voltage protection for insulated gate type bipolar transistors (IGBT). In the past, such protection was provided by avalanche diodes connected in parallel with the IGBT. The prior art

avalanche diode could, as shown in Figure 6 of the application, be embedded in the semiconductor structure of the IGBT or, alternatively, could be a discrete device externally connected in parallel with the IGBT. The onset of conduction in the avalanche diode clamps the voltage appearing between source and drain of the IGBT.

The inventors of the present invention were the first to realise that reverse over voltages can be clamped with a stable onset, thus protecting the IGBT device, by a combination of punch through across the base layer of the device and restriction of the junction area between the base and the drain.

None of this is evident from the prior art.

It is known from document D1 that, when subjected to a high enough electric field, a bipolar device displays avalanche breakdown or punch through, depending on the thickness of the base layer and its doping concentration. However, document D1 does not address the subject of device protection at all.

Document D2 discloses bipolar devices with different device parameters and breakdown voltages. Although calculation using the formulae of document D1 show that in some devices the avalanche breakdown voltage is higher than the punch through voltage, in other devices it is lower, and in any event there is no mention in the document of the problem of device protection.

Documents D3 and D5 disclose bipolar devices in which highly doped material is embedded between the first and second semiconductor layers. This is stated to improve the switching off speed of the device by injecting

carriers into the junction region between the first and second semiconductor layer. There is no indication given that such a layer would improve the switch-on current/voltage characteristics in an over voltage protection arrangement.

Reasons for the Decision

1. The appeal is admissible.
2. *Amendments*

Claim 1 of the request includes the following amendments compared to claim 1 as originally filed:

- (a) the subject-matter of original claim 2 has, with some editorial amendments, been incorporated into the claim as its characterizing clause.
- (b) the layer structure of the device and other features of the semiconductor device have been more specifically defined by incorporating further details derived from the description.

The description has been amended to acknowledge the cited prior art, to align the terminology of the description with that of the claims and to correct some linguistic errors.

The Board is satisfied that none of these amendments has introduced any new subject-matter extending beyond the content of the application as originally filed and, therefore, that the application complies with the requirements of Article 123(2).

3. *Novelty and inventive step*

3.1 The closest prior art document is document D2. The document compares the calculated output characteristics of bipolar transistors with measured ones, and lists in Table 1 several devices with different breakdown voltages for which the comparison was performed. The listed devices have base layers of different doping levels and thicknesses.

According to document D1, part of a well-known leading text and reference book in the field of semiconductors since well before the priority date of the invention, the avalanche breakdown voltage V_B for an abrupt junction is given by:

$$V_B = 5.34 \times 10^{13} (N_{n1})^{-0.75}$$

where N_{n1} is the doping concentration of the semiconductor layer concerned.

while the punch through voltage is given by:

$$V_{PT} = \frac{qN_{n1}W_{n1}^2}{2\epsilon_s}$$

where q is the electronic charge, ϵ_s the permittivity of the semiconductor material, and W_{n1} the width of the semiconductor region concerned. This formula is in substance identical to formula (3) of the description in the application in suit.

Applying these formulae to the devices listed in table 1 of document D2, they are shown to have avalanche breakdown voltages which in the case of the devices labelled A, C and I lie below, and in the case

of the devices labelled D, F und L lie above the corresponding punch through voltages. The appellant did not dispute during the oral proceedings that these findings are correct.

- 3.2 The invention claimed in claim 1 differs from the devices D, F, and L disclosed in document D2 by the features set out in the characterizing part of the claim. The claimed invention is therefore new.
- 3.3 The devices D, F and L of Figure 1 share with the claimed invention the property that the avalanche breakdown voltage lies above the punch through voltage, which therefore protects these devices against the adverse effects of avalanche breakdown. However, as shown in Figure 3 of the drawings accompanying the application in suit, conductivity modulation at the onset of punch through causes the drain current to fluctuate non-uniformly with the applied voltage.
- 3.4 The invention attempts to solve the problem of providing over voltage protection in an IGBT in which punch through occurs, such that the drain current at the onset of punch rises in a smooth and stable manner. The invention solves this problem by providing an embedded a region of highly doped semiconductor material at or near the junction between the base and the drain which prevents the formation of a conductivity modulated region (application as filed, page 6, line 27 to page 7, line 6; page 13, lines 9 to 18; Figures 2 and 4).
- 3.5 Document D1 is a well known text book which serves to illustrate the common general knowledge, at the priority date of the application in suit, of the skilled person in the art of semiconductor devices and, in particular, in the art of IGBTs and related structures. In addition to providing formulae for

calculating the avalanche breakdown and punch through voltages, document D1 also explicitly states that "Depending on the thickness of the n1 layer W_{n1} , the breakdown will be caused by avalanche multiplication if the depletion layer width at breakdown is less than W_{n1} , or caused by punch-through if the whole width W_{n1} is filled out first by the depletion layer ...". This passage shows that the person skilled in the art would, at the priority date of the invention, have understood the different breakdown modes of the devices A, C and I and D, F and L, respectively, of document D2. However, the skilled person would not have been aware from the contents of this document that protection of an IGBT against excessive reverse voltages could be achieved by embedding a highly doped region in the device structure which prevents the formation of a conductivity modulated region and thereby provides a smooth and stable onset of the reverse drain current on punch through.

- 3.6 Documents D3 and D5 relates to bipolar transistors of generally the same structure as the devices to which the invention relates. Documents D3 and D5 also disclose a highly doped layer similar to the n^+ layer 6 of the application in suit at the junction between the base and drain regions. However, in documents D3 and D5 the highly doped layer is provided to improve the switch-off performance of the device. According to document D5, the effect which brings about the improved switch off performance is the rapid removal of majority carriers from the active base region. There is no mention in either document of choosing device parameters such that the punch through voltage lies below the avalanche breakdown voltage or of employing such device structures in order to provide protection against excessive reverse voltages.

3.7 The purpose of the n+ region located at or in the vicinity of the base-drain junction is to restrict the conductivity modulated area (see paragraph 3.4 above). The Board accepts the appellant's argument that there is no reason to expect that the provision of this region in a bipolar device in which punch through is used to clamp excessive reverse voltages would provide a smooth and stable turn-on characteristic of the kind shown in Figure 4 of the application in suit.

3.8 For the foregoing reasons, in the judgement of the Board the invention as claimed would not be obvious from the cited prior art and therefore involves an inventive step as required by Articles 52(1) and 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal it is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

claims: 1 to 7 as filed at the oral proceedings

description: pages 2, 3, 3a, 3b, 4, 5, 9, 11, 13 and 14, as filed with the statement of the grounds of appeal
page 7 as filed during the oral proceedings
pages 1, 6, 8, 10 and 12 as originally filed;

drawings: sheets 1 to 5, Figures 1 to 6, as originally filed.

The Registrar:



U. Bultmann

The Chairman:



R. K. Shukla