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D E C I S I O N
of 30 October 2002

Case Number: T 0463/99 - 3.4.3

Application Number: 94400928.1

Publication Number: 0638931

IPC: H01L 23/538

Language of the proceedings: EN

Title of invention:
Multi-chip module

Applicant:
FUJITSU LIMITED

Opponent:
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Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Novelty and inventive step (yes) (after amendments)"
"Distinguishing features of the invention contrary to the essential features of the closest prior art"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0463/99 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 30 October 2002

Appellant: FUJITSU LIMITED
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Representative: Joly, Jean-Jacques
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Decision under appeal: **Decision of the Opposition Division of the European Patent Office dated 28 December 1998 revoking European patent No. 0 638 931 pursuant to Article 102(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. J. Vogel

Summary of Facts and Submissions

I. The European patent application No. 94 400 928.1 (Publication No. 0 638 931) was refused by the examining division by a decision dated 28 December 1998 on the ground that the subject-matter of the main request was not new having regard to document

D2: US-A-5 130 768.

Claim 1 of the main request had the following text:

"A multi-chip module comprising:

a base board (30);

a wiring board (18) facing a first surface of said base board over the entire surface thereof;

a thin-film multi-layer circuit board (32) which is provided on said first surface of the base board and has a multi-layer structure in which insulating layers (32B-1 to 32B-5) and wiring conductors (32A-1 to 32A-5) are stacked, wherein said thin-film multi-layer circuit board includes at least one of said wiring conductors which is exposed from an outermost insulating layer (32B-5) at a main external surface of said board (32), said exposed wiring layer (32A-5) defining connection pads;

circuit elements (14, 16) attached to connection pads on said main external surface of the thin-film multi-layer circuit board; and

terminals (34) which are attached to the main external surface of the thin-film multi-layer circuit board and electrically connect the said connection pads to circuits formed on a wiring board on which the multi-chip module is mounted,

so that the terminals are attached and supported between said connection pad of the thin-film multi-layer circuit board and said circuits on said wiring board (18)."

There were additional comments in the above decision which concerned two auxiliary requests which were found to lack an inventive step having regard to the same document D2 and a third auxiliary request which was considered as involving an inventive step if amended for clarity.

II. The applicant lodged an appeal against this decision on 4 March 1999 paying the appeal fee on the same day. A statement setting out the grounds of the appeal was filed on 21 April 1999 together with three sets of amended claims forming the basis of a main request and first and second subsidiary requests respectively.

III. In its communication dated 25 April 2002, the Board informed the appellant (applicant) that claim 1 of the main request did not appear to involve an inventive step within the meaning of Article 56 EPC, and that claim 6 of respectively the first and second auxiliary request was not clear.

The appellant filed a new set of claims on 16 September 2002 and an amended page 4 on 14 October 2002 and requested that the decision under appeal be set aside

and a patent be granted on the basis of the following patent application documents:

Description:
Pages 1 to 3, 7 to 9 and 12 as filed;
Page 4, filed with letter dated 14 October 2002;
Page 5 filed with letter dated 30 December 1996;
Pages 6, 10 and 11 filed with letter dated 16 September 2002;

Claims:
Nos. 1 to 14 filed with letter dated 16 September 2002;

Drawings:
Sheets 1/8 to 5/8 as filed;
Sheets 6/8 to 8/8 filed with letter dated 16 September 2002.

Claim 1 of the appellant's request is the only independent claim of the set of 14 claims and reads as follows:

"A multi-chip module comprising:

a base board (30);

a thin-film multi-layer circuit board (32) which is provided on a first surface of the base board, **which is supported by said base board** (30) and has a multi-layer structure in which insulating layers (32B-1 to 32B-5) and wiring conductors (32A-1 to 32A-5) are stacked, wherein said thin-film multi-layer circuit board includes at least one of said wiring conductors which is exposed from an outermost insulating layer (32B-5) at a main external surface of said thin-film multi-

layer circuit board (32), said exposed wiring layer (32A-5) defining connection pads;

circuit elements (14, 16) **mounted** on said main external surface of the thin-film multi-layer circuit board **and electrically connected to connection pads thereof**;

terminals (34) which are attached to said main external surface of the thin-film multi-layer circuit board **for electrically connecting the** said connection pads to circuits formed on a wiring board on which the multi-chip module is to be mounted;

said terminals extending beyond a top surface of said circuit elements facing away from said main external surface of the thin-film multi-layer circuit board (32) so that said circuit elements (14, 16) are facing said wiring board but not contacting it."

Features which particularly distinguish the above claim 1 from the claim forming the basis of the appealed decision have been emphasised by the Board.

IV. The appellant submitted the following arguments in support of his request:

Claim 1 is based on a text corresponding to the auxiliary request which was found allowable by the examining division.

The object of the present invention is to provide a high-density, high speed multi-chip module having high flexibility in the design and production which is less expensive than the prior art modules.

Document D2 discloses a micro-chip module comprising a thin-film multi-layer board which is covered with a relatively thick insulative layer provided with openings used as solder wells for inserting therein the ends of the terminals; these openings and thus the insulative layer have the functions of stabilizing the pins inserted in the substrate and they refrain the flow of solder and the movement of chip during heating of the substrate.

A microchip module without an insulating layer and solder wells was, therefore, not obvious to the skilled person. This measure however allows to achieve the object of the invention as mentioned above. Therefore, the subject-matter of claim 1 involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of the amendments*

The present application concerns multi-chip modules with a stacked structure comprising a wiring board (18), a base board (30) attached to a thin film multi-layer circuit board (32), circuit elements being mounted and connected on the main surface of the thin film multi-layer circuit board facing the wiring board (18); terminals (34) separate and hold together the wiring board (18), on the one hand, and the surface of the thin-film multi-layer circuit board carrying the circuit elements, on the other hand, so that the circuit elements (14) do not contact the surface of the

wiring board (18). Electrical connections are provided so that wirings of the wiring board are connected to the circuit elements (14) over the terminals (34). The base board (30) is attached to the main surface of the thin-film multi-layer circuit board which is opposite to the main surface carrying the circuit elements, and thus opposite to the wiring board (18).

Such a multi-chip module is disclosed in the application as filed with reference to claim 1 and the common constructional features of the embodiments illustrated by the original Figures 4 to 9 and 11 to 15.

The dependent claims 2 to 14 correspond to the information disclosed in the dependent claims 2 to 12 and the particular features derivable from the different embodiments illustrated by the above Figures of the application as filed.

The description relating to the embodiment illustrated by original Figure 10, and Figure 10, concern a multi-chip module wherein the circuit elements mounted on a main surface of the thin-film multi-layer circuit board are not located between the base board and the wiring board, as claimed in the present claim 1. Figure 10 and the corresponding description have been deleted, and the original Figures 11 to 15 have been renumbered accordingly.

Therefore, in the Board's judgment, the present application satisfies the requirement of Article 123(2) EPC that a European patent application may not be amended in such a way that it contains subject-matter extending beyond the content of the application as

filed.

3. *Clarity of the claims*

The Board is satisfied that, with the amendments provided by the appellant, the application complies with the requirements of clarity of the claims and support by the description of Article 84 EPC.

4. *Novelty*

4.1 A multi-chip module is known from document D2 (see in particular the text corresponding to Figure 4) comprising:

a base board, i.e., the base layer of the daughter substrate (12), with a main surface (16) constituting one main external surface of both the daughter substrate (12) and the multi-chip module (see also column 3, line 63 to column 7, line 29, and Figure 3);

on the opposite main surface of the base board and in contact therewith, **a further board**, which is also a part of the daughter substrate (12) which is supported by the base board, **comprises** a thin-film multi-layer circuit board having a multi-layer structure in which insulating layers and wiring conductors (17, 56) are stacked; the thin-film multi-layer circuit board includes at least one of said wiring conductors (17, 56) which is exposed from an outermost insulating layer at the main external surface of the thin-film multi-layer circuit board facing away from the base board; the exposed wiring layer (17, 56) defines connection pads (17, 56) (see also column 6, line 63 to column 7, line 6; column 7, lines 17 to 29 and 45 to 55, and

Figure 3);

circuit elements (40), i.e. chips (40), mounted on this same main external surface of the thin-film multi-layer circuit board of the daughter board (12) comprising the connection pads (17, 56), these circuit elements being electrically connected to connection pads (56) of the thin-film multi-layer circuit board; and

terminals (88) which are attached to the same main external surface of the thin-film multi-layer circuit board of the daughter substrate (12) comprising the connection pads (17, 56), for electrically connecting these connection pads to circuits formed on the surface of a mother substrate (22) facing the circuit elements (40) and this same main external surface of the thin-film multi-layer board; the mother substrate having the function of a wiring board on which the multi-chip module is mounted.

4.2 However, the micro-chip module known from Figure 4 of document D2 additionally comprises **a relatively thick layer of insulative material** (59) disposed upon the main external surface of the thin-film multi-layer circuit board and provided with apertures (15) for exposing the connection pads (17, 56) in the thin-film multi-layer circuit board.

In other words, the further board, while comprising a thin-film multi-layer circuit board, is not a thin-film multi-layer circuit board. The connection pads (56, 17) are exposed from an outermost insulating layer (59) of the further board which is on a main external surface of the thin-film multi-layer circuit board, but which is not part of the thin-film multi-layer circuit board.

Moreover, in the known micro-chip module, the terminals (88) do **not** extend beyond a top surface of the circuit elements (40) facing away from the main external surface of the thin-film multi-layer circuit board of the daughter board (12).

Additionally, these circuit elements (40) facing the wiring board of the mother board (22) are in contact with the supporting part (50, 35) of the mother board, i.e. of the wiring board.

4.3 The further prior art documents cited in the decision under appeal are less relevant.

4.4 Therefore, the subject-matter of claim 1 is new in the sense of Article 54 EPC.

5. *Inventive step*

5.1 According to the present application (see in particular page 4, lines 24 to 30), an object of the present invention is to provide a high-density, high speed multi-chip module having high flexibility in the design and production which is less expensive than the prior art modules.

5.2 The following is to be noted concerning the first distinguishing feature:

As convincingly argued by the appellant, in the multi-chip module known from document D2 a relatively thick layer (59) of insulative material is disposed on the main surface of the daughter substrate (12) facing the mother board and the connection pads are exposed through openings provided in the relatively thick

insulating layer. It is necessary in the known technique to control the introduction of the ends of the terminals (88) and also those of the terminals (80) connecting directly the circuit elements (40) or chips (40) into the corresponding holes in the relatively thick insulating layer (59) of the daughter board. For the presently claimed device, it is not necessary to provide a relatively thick insulating layer with openings which act as solder wells during the soldering of the terminals (80, 88).

The following is to be noted concerning the two further distinguishing features, which were explicitly or implicitly contained in claim 1 of the third auxiliary request which had been considered by the examining division as containing patentable subject-matter:

In the presently claimed devices, wherein the terminals (34) extend beyond a top surface of the circuit elements (40) facing away from the main external surface of the thin-film multi-layer circuit board of the daughter board (12) and wherein these circuit elements (40) do not contact the wiring board, the design flexibility of the thin-film multi-layered circuit board of low cost production is credibly achieved.

On the other hand, in document D2 (see column 3, lines 3 to 14), it is specified that the surface (42) of a circuit element (40), facing away from the thin-film multi-layer circuit board (12) is affixed to and is in intimate thermal conductive relation with part of the mother board, i.e., the wiring board, and, in the embodiment of Figure 4, these parts are in contact. Thus, the terminals (88) from the thin-film multi-layer

board to the wiring board do not need to extend beyond the top surface of the circuit elements (40) in contact with the wiring board, and this is shown accordingly.

5.3 In view of the above, the features distinguishing the claimed multi-chip module from document D2 are contrary to the essential features of the module disclosed in the document and cannot be regarded as obvious.

The further prior art documents were not considered relevant in the decision under appeal and the Board is satisfied that they do not render the claimed module obvious.

Therefore, in the Board's judgment, having regard to the state of the art, the subject-matter of claim 1 is not obvious to a person skilled in the art and thus involves an inventive step in the sense of Article 56 EPC.

Consequently, claim 1 and the dependent claims, which concern particular embodiments of claim 1, are patentable in the sense of Article 52(1) EPC, so that a patent can be granted on this basis.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside;

2. The case is remitted to the department of first instance with the order to grant a patent with the following patent application documents:

Description:

Pages 1 to 3, 7 to 9 and 12 as filed;
Page 4, filed with letter dated 14 October 2002;
Page 5 filed with letter dated 30 December 1996;
Pages 6, 10 and 11 filed with letter dated 16 September 2002;

Claims:

Nos. 1 to 14 filed with letter dated 16 September 2002;

Drawings:

Sheets 1/8 to 5/8 as filed;
Sheets 6/8 to 8/8 filed with letter dated 16 September 2002.

The Registrar: The Chairman:

P. Martorana R. K. Shukla