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D E C I S I O N
of 15 December 2000

Case Number: T 0189/99 - 3.5.1

Application Number: 93303466.2

Publication Number: 0569218

IPC: G06F 12/02

Language of the proceedings: EN

Title of invention:
Circuit for rotating a digital image

Applicant:
XEROX CORPORATION

Opponent:
-

Headword:
Circuit for rotating a digital image/XEROX CORPORATION

Relevant legal provisions:
EPC Art. 56, 52(1)

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
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Case Number: T 0189/99 – 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 15 December 2000

Appellant: XEROX CORPORATION
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                                        New York 14644 (US)

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Decision under appeal: **Decision of the Examining Division of the**
                               European Patent Office posted 17 November 1998
                               refusing European patent application
                               No. 93 303 466.2 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: R. Randes
                 P. H. Mühlens

Summary of Facts and Submissions

I.   This is an appeal against the decision of the Examining
        Division to refuse European Patent Application
        93 303 466.2 because the subject matter of claim 1
        lacked inventive step having regard to the prior art
        acknowledged in figure 6 of the application itself,
        derived from

        D2: EP-A-0 433 645,

        and the disclosure of the following document:

        D1: EP-A-0 276 110.

II.   The Appellant (Applicant) has requested grant of a
        patent and made an auxiliary request for oral
        proceedings.

III.   The Appellant requests grant of a patent based on the
        following documents:

        Claim:
        1 received on 10 October 2000

        Description:
        Pages 1-3 received on 29 September 1998
        Pages 4-5 received on 17 October 1997

        Drawings:
        Page 2/5 as originally filed
        Pages 1/5 and 3/5 to 5/5 received on 17 October 1997.

IV.   Claim 1 reads as follows:

"A circuit for addressing one bit at a time in a random
access memory device (14) having x address lines
divided into column address lines and row address
lines, the circuit comprising:

    an x bit counter (10) having y least significant
bits, z most significant bits, and n intermediate bits,
where y + z + n = x, and x, y, z and n are positive
integers,
    a first multiplexer (12) connected to the counter
(10) and having A and B inputs and an output, the A and
B inputs being connected to the counter (10) with the A
input being coupled to the y least significant bits and
the B input being coupled to the z most significant
bits;
    a second multiplexer (13) connected to the counter
(10) and having A' and B' inputs and an output, the A'
and B' inputs being connected to the counter (10) with
the A' input being coupled to the z most significant
bits and the B' input being coupled to the y least
significant bits; and
    a register (11) having y + z + n input and output
lines wherein the y least significant of the input
lines (A0 - A8) thereof are coupled to the output of
the first multiplexer (12), the n intermediate input
lines (A9 - A12) thereof are coupled to the n
intermediate bits (C9 - C12) of the counter (10) and
the z most significant of the input lines (A13 - A21)
thereof are coupled to the output of the second
multiplexer (13), wherein the multiplexers (12, 13) in
a first state couple the A and A' inputs to the
register (11) and in a second state couple the B and
B', inputs to the register (11);
    characterised in that the y least significant bit
(A0 - A8) output lines of the register (11) are divided

into lower least significant bit (A0 - A5) output lines
and upper least significant bit (A6 - A8) output lines,

the z most significant bit (A13 - A21) output
lines of the register (11) are divided into lower most
significant bit (A13 - A17) output lines and upper most
significant bit (A18 - A21) output lines,

said lower least significant bit (A0 - A5) output
lines and said lower most significant bit (A13 - A17)
output lines being coupled to the column address lines
of the random access memory device (14),

said upper least significant bit (A6 - A8) output
lines, the intermediate bit (A9 - A12) output lines and
said upper most significant bit (A18 - A21) output
lines of the register (11) being coupled to the row
address lines of the random access memory device (14)."

Reasons for the Decision

1.   *Admissibility*

The appeal is admissible.

2.   *Background*

Memories for storing and rotating digital images are
usually organised as two-dimensional arrays, each
memory location being specified by a row address and a
column address. If such memories are addressed in such
a way that consecutive locations differ only in their
column address then faster reading and writing is
achievable in what is known as the "fast page mode" of
accessing. If an image is merely stored in such a
memory and then read out again, then fast page mode
addressing is possible for both writing and reading. If

however the image is also to be rotated then data is
written into the memory in one "direction", but read
out of the memory in another "direction". For instance,
when writing data into the memory consecutive locations
usually differ only in their column address so that
fast page mode accessing is possible. However when
reading data out of the memory consecutive locations
usually differ only in their row address so that fast
page mode accessing is not possible. As a consequence
fast page mode accessing is only possible for reading
or writing, but not both. This leads to the undesirable
result that memory access for image storage occurs at a
different rate to memory access for image storage with
rotation. The invention overcomes this problem by
providing a circuit for addressing which rearranges the
memory row and column address lines to change the way
in which an image is mapped onto the two-dimensional
memory area with the result that fast page mode
accessing is, at least partly, possible in both
directions.

3.   *Amendments*

In addition to editorial amendments and the correction
of errors pointed out by the Examining Division in its
decision, claim 1 has been amended with respect to the
refused version by the addition in the first line of
the expression "one bit at a time in" and the addition
in the final paragraph of the expression "the
intermediate bit (A9 - A12) output lines", these
features having been discussed in paragraph 15.2 of the
impugned decision. Since these amendments are supported
by column 1, lines 50-53 and figure 7 of the published
application, the new claim satisfies Article 123(2)
EPC. The claim is also clear and supported by the

description.

4.   *Novelty*

It is common ground between the Appellant and the Board
that the prior art acknowledged in figure 6 of the
application represents the closest prior art on file.
The Appellant has stated that, even though D2 does not
contain a figure corresponding to figure 6 of the
application, figure 6 gives a view of the prior art
known from D2.

Figure 6 of the application discloses the features set
out in the preamble of claim 1 for the case $x=22$, $y=9$,
$n=4$, $z=9$. Since the characterising features of claim 1
are not disclosed by figure 6 of the application, the
subject matter of claim 1 is novel over this prior art.

D1 concerns the storage of an image having three
dimensions (X,Y and S) in a memory which, in response
to a row address (RA0-RA7), outputs a complete row of
data consisting of several data words. D1 seeks to
solve the problem that although data can be read
quickly in the X direction by accessing a row at a
time, access in the S and Y direction is slow since
each bit is in a different row. The solution lies in
each row containing data words relating to all three
dimensions. Hence data can be read for all directions
by reading a row and selecting the appropriate word.
This selection is made based on the settings of the B0-
B1 and C0-C3 address lines which can thus be regarded
as column address lines (see fig. 17). The row and
column addresses are generated from external row and
column addresses (Y0-Y8 and X0-X8) by the address
scramble circuit (50) which is shown in figures 17 and

19 and described by truth tables 6-1 and 6-2.

Hence the address scramble unit (50) of D1 in the
X-access mode rearranges memory address lines in a
similar way to that set out in the characterising part
of claim 1. However D1 does not relate to addressing
one memory bit at a time, as required by claim 1.
Instead D1 is concerned with addressing one word at a
time. Consequently D1 does not mention any intermediate
bits and the four least significant external column
address bits (X0-X3) are not used by the address
scramble unit in X-access mode; see page 13, lines
33-36. Since a circuit for addressing one bit at a time
in a random access memory device is not disclosed by
D1, the subject matter of claim 1 is also novel over
D1.

The Board notes that the remaining document cited in
the European Search Report (GB-A-2 092 785) merely
reflects background art.

5.   *Inventive step*

The subject matter of claim 1 differs from the prior
art shown in figure 6 of the application in the
features set out in the characterising part of claim 1.
These differences have the effect of allowing fast read
mode to be used when reading out from the memory both
horizontally and vertically and result from solving the
technical problem of increasing access speeds in the
direction in which fast page mode cannot be used.

The impugned decision states in paragraph 13 that the
skilled person confronted with this problem would
certainly consult D1 which is in the same technical

field of memories for image processing. Whilst it is
true that D1 and D2 belong to the same technical field,
the Board is unconvinced for two reasons that the
skilled person would regard D1 as offering a solution
to the above problem. Firstly, D2, like the circuit set
out in claim 1, concerns the addressing of a memory one
bit at a time, whilst D1 relates to a memory in which
16-bit words are addressed (see fig. 17; DQ0 - DQ15).
Secondly, D1 does not mention intermediate bits and so
cannot indicate what should be done with the
intermediate bits shown in figure 6 of the application.
Claim 1 however makes clear how these intermediate bits
are used.

Moreover, as argued by the Appellant, the hypothetical
application of the teaching of D1 to the circuit shown
in figure 6 of the application does not result in the
subject matter of the claim, since the address scramble
unit known from D1 converts eighteen external address
lines into fourteen internal address lines, thus not
using the four least significant X address lines. The
result would consequently be the use of only fourteen
of the eighteen counter (10) bits to address the memory
(14). This possibility does not however fall within
claim 1 which requires that the number of memory
address lines (x) be equal to the number of bits of the
counter (10). The Board can furthermore see no obvious
reason for the skilled person to further modify the
circuit to also use the four least significant counter
bits.

6.   The Board concludes that the subject matter of claim 1
        involves an inventive step, Articles 52(1) and 56 EPC.

7.   *Deficiencies*

Although claim 1 is allowable, the description requires
adaption to the wording of claim 1 to comply with Rule
27(1)(c) EPC. Moreover the reference symbols "A'" and
"B'" used in the claim cannot be found in the figures,
particularly figure 7, contrary to Rule 32(2)(i) EPC.
The Board consequently remits the case to the Examining
Division to attend to these deficiencies.

8.   *Oral proceedings*

Since the Appellant's request is allowable, oral
proceedings, mentioned at point II above, need not be
held.

Order

For these reasons it is decided that:

1.   The decision is set aside.

2.   The case is remitted to the Examining Division with the
      order to remove the deficiencies mentioned in paragraph
      7 above and to grant a patent on the basis of the
      Appellant's request (see paragraph III above).

The Registrar: The Chairman:

M. Kiehl   P. K. J. van den Berg

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