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D E C I S I O N
of 21 December 2000

Case Number: T 0096/99 - 3.5.2

Application Number: 94202212.0

Publication Number: 0639006

IPC: H03K 19/173

Language of the proceedings: EN

Title of invention:
Multiplexed control pins for in-system programming and boundary scan testing using state machines in a high density programmable logic device

Applicant:
LATTICE SEMICONDUCTOR CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Novelty (yes)"
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0096/99 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 21 December 2000

Appellant: LATTICE SEMICONDUCTOR CORPORATION
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 5 August 1998 refusing European patent application No. 94 202 212.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: M. R. J. Villemin
B. J. Schachenmann

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 94 202 212.0. The reason given for the refusal was that the subject-matter of the claims then on file did not involve an inventive step, having regard to the prior art shown in Figure 3 of the application and the following prior art documents:

D2: US-A-4 602 210

D3: WO-A-92/20157.

II. In reply to a communication of the Board, the appellant filed with a letter dated 8 December 2000 a set of amended claims 1 to 13, an amended page 4 of the description and amended Figures 4 and 6.

III. Claim 1 is now worded as follows:

"An in-system programmable logic device comprising a common interface for accessing boundary scan testing and in-system programming functions, including a first pin (1) for receiving an enable signal (ISPEN), said enable signal (ISPEN) having a first state and a second state, said first state enabling in-system programming of said device and said second state enabling a boundary-scan test function of said device, said in-system programmable logic device further comprising:

a second pin (3) for receiving a mode input signal (MODE) for performing in-system programming when said enable signal (ISPEN) is in said first state, said second pin (3) receiving a test mode select signal (TMS) for performing a boundary-scan test function when said enable signal (ISPEN) is in said second state;

a third pin (4) for receiving a serial data input signal (SDI) for performing in-system programming when said enable signal (ISPEN) is in said first state, said third pin (4) receiving a test data input signal (TDI) for performing a boundary-scan test function when said enable signal (ISPEN) is in said second state;

a fourth pin (2) for receiving a shift clock signal (SCLK) for performing in-system programming when said enable signal (ISPEN) is in said first state, said fourth pin (2) receiving a test clock signal (TCK) for performing a boundary-scan test function when said enable signal (ISPEN) is in said second state; and

a fifth pin (5) for providing a serial data output (SDO) signal for performing in-system programming when said enable signal (ISPEN) is in said first state, said fifth pin (5) providing a test data output (TDO) signal for performing a boundary-scan function when said enable signal (ISPEN) is in said second state."

Claim 8 concerns a method for controlling an in-system programmable logic device. Claims 2 to 7 are dependent on claim 1. Claims 9 to 13 are dependent on claim 8.

IV. In the notice setting out the statement of grounds of appeal the appellant argued essentially that the present invention achieved a synergistic effect not achieved in the prior art by assigning similar signals in in-system programming and boundary scan operation to the same pins. Documents D2 and D3 did not teach or suggest a pin-assignment exploiting the similarity of signals between boundary scan testing and in-system programming.

V. The appellant requested that the decision under appeal be set aside. Although not expressly stated by the appellant, it is implicit that the appellant further requests that a patent be granted on the basis of the application in its present form, namely:

Claims: 1 to 13 filed with the letter dated 8 December 2000.

Description: Pages 1, 5 to 9, 11 to 15 as originally filed; page 2 as filed with the letter dated 28 February 1997;
pages 3 and 10 as filed with the letter dated 3 September 1997; page 4 as filed with the letter dated 8 December 2000.

Drawings: Figures 1, 2, 3, 5a, 5b as filed with the letter dated 15 November 1994;
Figures 4 and 6 as filed with the letter dated 8 December 2000.

Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of the amendments*

- Reference numerals have been introduced in the claims to comply with Rule 29(7) EPC.

- In claim 1, it has been clarified that the second pin (3) receives a test mode select signal (TMS) for performing a boundary-scan test function when the enable signal (ISPEN) is in said second state, and an obvious clerical error has been corrected.

- In Figure 4, the legend in box 14 has been corrected to "OUTPUT MUX" in conformity with page 6, lines 20 and 21, of the application as filed.

- In Figure 6, "N-Bit CLB Reg" has be corrected to "N-Bit GLB Reg", in conformity with page 12, lines 8 and 9, of the application as filed.

- an acknowledgement of the prior art disclosed in D2 has been introduced on page 4 of the description to comply with Rule 27(1)(b) EPC.

The features recited in the amended set of claims 1 to 13 were all disclosed in the application as originally filed. In the judgement of the Board, the present amended form of the application does not infringe Article 123(2) EPC, and the claims satisfy the requirements of Article 84 EPC.

3. *Novelty*

Neither of the prior art documents D2 and D3 discloses all the features recited in independent claims 1 and 8. Thus, the subject-matter of the claims is novel within the meaning of Article 54 EPC.

4. *Inventive step*

4.1 Starting from the prior art according to Figure 3 of the present application, the present application addresses the problem of reducing the number of pins required for in-system programming and boundary-scan testing in an integrated circuit package (see page 3, lines 10 to 21 of the original description). According to claim 1, the logic device comprises a common interface for accessing boundary-scan testing and in-system programming functions. This is obtained by providing a first pin (1) which receives an enabling signal (ISPEN) as shown in Figure 4 for enabling either

an in-system programming function or a boundary-scan test function to be carried out. According to the logical state of this enabling signal, the same second, third, fourth and fifth pins (pins 3, 4, 2 and 5, Figure 4) are shared to perform either an in-system programming operation (signals MODE, SDI, SCLK and SDO) or a boundary-scan testing operation (signals TMS, TDI, TCK and TDO) of the claimed logic device.

4.2 The problem of reducing the number of pins by sharing of the same set of pins for mission inputs/outputs and test data inputs/outputs is known from document D2 (see column 1, lines 35 to 42) and solved by the logic device disclosed in that document (see description column 1, lines 6 to 11; column 3, lines 36 to 40 and Figures 7 to 9).

4.2.1 The logic device disclosed in D2 has several features in common with the in-system programmable logic device defined in claim 1 of the present application. In particular, the "mission (i.e. functional) mode", defined in D2 at column 4, lines 43 and 44, corresponds to the "in-system programming" according to the present application.

Referring to Figure 8 of D2, it can be seen that a plurality of n input pins PI are used for entering either mission signals through mission logic 30 or test signals through scan paths SP_1-SP_p into the logic device according to the value of a signal XS (corresponding to signal ISPEN shown in Figure 4 of the present application). The signal XS is applied to an input demultiplexer 28 and to an output multiplexer 34.

4.2.2 It is indicated in D2 (column 3, lines 36 to 40) that the scan path inputs and outputs are multiplexed with the mission primary inputs and outputs, "and consequently there are no additional pin requirements for scan path inputs and outputs". However, the Board observes that:

- the choice of signals to be assigned to the second, third and fourth pins according to claims 1 and 8 of the present application is not disclosed in D2,

- it is not disclosed in D2 that according to the logical states of the signal XS, a second, a third, a fourth and a fifth pin are shared to perform either a mission function or a test function. In particular, the output multiplexer 34 has a plurality of m output pins and it is not indicated that this plurality of pins could be reduced to a single pin (corresponding to the fifth pin (5) of the present application) for providing a serial data output signal for performing either a mission function or a test function according to the logic state of the XS signal.

4.3 Document D3 discloses the use in a logic device of a common interface for accessing either in-system programming or another (unspecified) function on normal input or output lines, in order to reduce the number of input or output lines (see page 2, lines 17 to 33; page 5, line 27 to page 6, line 2).

4.3.1 This known device is provided with an input pin for receiving an enable signal (for example, $\overline{ISP}$ in Figures 2A, 2B' and 6 and ISPEN in Figure 2C'), the logical state of which determines the function to be performed. Referring to Figure 2A and page 4 of the description of D3, it is indicated that input pins I_0 to I_3 also serve "as in-system programming (ISP) pins when the signal on the ISP pin is asserted" (see also claim 1 of D2).

4.3.2 However, the features of the present invention lacking in the logic circuit of D2 (see paragraph 4.2.2 above) are neither disclosed nor hinted at in D3.

5. Summarizing, the prior art shown in Figure 3 of the present application and the prior art disclosed in documents D2 and D3 does not render it obvious to the skilled person to provide an in-system programmable logic device comprising the combination of features specified in claim 1, or a method of controlling an in-system programmable logic device comprising the combination of features specified in claim 8.

The subject-matter of claims 1 and 8 is therefore considered as involving an inventive step within the meaning of Article 56 EPC.

6. However, the Board has noticed that the embodiment described with reference to Figure 6 and claimed in dependent claims 3 to 7 and 10 to 13 does not have a "first pin" for receiving an enable signal (ISPEN). It appears that such a pin may not be necessary (cf page 5, lines 4 to 7 of the published application). This matter, which was not raised by the first instance, needs to be clarified before a patent could be granted. The Board therefore makes use of its power under Article 111(1) EPC to remit the case for further prosecution.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution, having regard to paragraphs 5 and 6 of the reasons.

The Registrar: The Chairman:

M. Hörnell W. J. L. Wheeler