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D E C I S I O N
of 10 October 2000

Case Number: T 1067/98 - 3.5.2

Application Number: 92907312.0

Publication Number: 0570529

IPC: G11C 7/00

Language of the proceedings: EN

Title of invention:
Refresh control arrangement for dynamic random access memory system

Applicant:
TM Patents L.P.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 84, 113(2)

Keyword:
"Claims not clear"

Decisions cited:
T 0032/82

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1067/98 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 10 October 2000

Appellant: TM Patents L.P.
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Boston, MA 02110 (US)

Representative: Grünecker, Kinkeldey,
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 12 May 1998 refusing European patent application No. 92 907 312.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: A. G. Hagenbucher
B. J. Schachenmann

Summary of Facts and Submissions

I. The appellant contests the decision of the Examining Division to refuse European patent application No. 92 907 312.0. The reason given for the refusal was that claims 1 and 12 filed 10 November 1997 did not meet the requirements of Article 84 EPC and, moreover, that those claims did not meet the requirements of Article 52(1) in conjunction with Articles 54 and 56 EPC. Although the applicant alleged there were differences over the prior art, they were not reflected in the independent claims. The following prior art documents were referred to in the decision under appeal:

D1: IBM Technical Disclosure Bulletin, volume 16, no. 3, August 1973, pages 934 to 936,

D2: US-A-4 357 686,

D3: WO-A-8 605 917 and

D4: US-A-4 185 323.

II. With the statement of grounds of appeal the appellant filed as a main request new claims 1 and 12 (titled "main request") to be prosecuted together with dependent claims 2 to 11 as on file (i.e. as filed on 10 November 1997) and as an auxiliary request claims 1 and 12 (titled "auxiliary request") to be prosecuted together with the dependent claims 3 to 11 as on file.

If the Board considered neither the main request nor the auxiliary request to be allowable, oral proceedings were requested.

III. Claims 1 and 12 of the main request read as follows:

"1. A memory controller for use in a digital computer system having a bus, the memory controller controlling a memory including a plurality of storage locations, said memory controller receiving memory access requests over the bus in the digital computer system for initiating a memory access operation in connection with a storage location in a selected bank, said memory controller comprising:

A. a memory access control circuit for receiving memory access requests over the bus and for performing a memory access operation in connection with a storage location in response thereto and initiating a refresh operation with respect to selected ones of said memory banks; and

B. a memory refresh control circuits for initiating a refresh operation with respect to selected ones of said memory banks comprising:

i. a refresh timer for generating a refresh timing signal to indicate an end of each of a succession of predetermined refresh time intervals;

ii. a concurrent refresh control circuit connected to said refresh timer and said memory access control circuit for enabling said memory access control circuit to initiate a refresh operation in connection with a selected memory bank following the generation of the refresh timing signal

concurrent with the performance by said memory access control circuit of a memory access operation, said concurrent rebank other than a memory bank with which the memory access control means is performing a memory access operation, said concurrent refresh control circuit maintaining a concurrent refresh status information indicating refresh status of each said memory bank; and

iii. an urgent refresh control circuit connected to said refresh timer, said memory access control circuit and said concurrent refresh control circuit for enabling said memory access control circuit to initiate a refresh operation in response to generation of the refresh timing signal and the concurrent refresh status information maintained by said concurrent refresh control circuit, in connection with a plurality of memory banks with respect to which said concurrent refresh control circuit did not initiate a refresh operation during the preceding timing interval and for concurrently disabling said memory access control means from performing a memory access operation, except for said refresh operation.

12. A method for operating a memory controller for use in a digital computer system having a bus, the memory controller for controlling a memory including a plurality of memory banks, each memory bank including a plurality of storage locations, said memory controller receiving memory access requests over the bus in the

digital computer system for initiating a memory access operation in connection with a storage location in a selected bank, said method comprising the steps of:

A. receiving memory access requests over the bus and performing a memory access operation in connection with a storage location in response thereto;

B. generating a timing signal to indicate an end of each of a succession of predetermined time intervals;

C. initiating a concurrent refresh operation in connection with a selected memory bank following the generation of the timing signal concurrent with the performance of a memory access operation, the concurrent refresh operation being initiated in connection with a memory bank other than a memory bank with which the memory access operation is being performed, and maintaining concurrent refresh status information indicating refresh status of each said memory bank; and

D. determining in response to a timing signal and the concurrent refresh status information the refresh status of each said memory bank and initiating an urgent refresh operation in response to generation of the timing signal in connection with a memory bank which was not refreshed by concurrent refresh operations during the preceding timing interval, and disabling said memory access operations during said urgent refresh operation, except for performing said refresh operation."

Claims 1 and 12 of the auxiliary request read as

follows:

"1. A memory controller for use in a digital computer system having a bus, the memory controller controlling a memory including a plurality of storage locations, said memory controller receiving memory access requests over the bus in the digital computer system for initiating a memory access operation in connection with a storage location in a selected bank, said memory controller comprising:

A. a memory access control circuit for receiving memory access requests over the bus and for performing a memory access operation in connection with a storage location in response thereto and initiating a refresh operation with respect to selected ones of said memory banks; and

B. a memory refresh control circuits for initiating a refresh operation with respect to selected ones of said memory banks comprising:

i. a refresh timer for generating a refresh timing signal to indicate an end of each of a succession of predetermined refresh time intervals;

ii. a concurrent refresh control circuit connected to said refresh timer and said memory access control circuit for enabling said memory access control circuit to initiate a refresh operation in connection with a selected memory bank following the generation of the refresh timing signal concurrent with the performance by said

memory access control circuit of a memory access operation, said concurrent rebank other than a memory bank with which the memory access control means is performing a memory access operation, said concurrent refresh control circuit maintaining a concurrent refresh status information indicating refresh status of each said memory bank; and

iii. an urgent refresh control circuit connected to said refresh timer, said memory access control circuit and said concurrent refresh control circuit for enabling said memory access control circuit to initiate a refresh operation in response to generation of the refresh timing signal and the concurrent refresh status information maintained by said concurrent refresh control circuit, in connection with a plurality of memory banks with respect to which said concurrent refresh control circuit did not initiate a refresh operation during the preceding timing interval and for concurrently disabling said memory access control means from performing a memory access operation, except for said refresh operation;

and, further comprising a memory bank control signal generating circuit for generating memory bank control signals for controlling said memory bank during a memory operation and refresh operation;

C. said memory access control circuit generating a

signal identifying a memory bank with which it is performing a memory access operation;

D. said concurrent refresh control circuit includes;

i. a concurrent refresh status circuit for generating concurrent refresh status indications for said memory banks in response to generation of said timing signal; and

ii. a concurrent refresh priority circuit for selecting a memory bank with which to initiate a refresh operation in response to the concurrent refresh status indications generated by said concurrent refresh status circuit for said memory banks and the memory bank identified by the signal from said memory access control circuit to thereby identify a memory bank with which a refresh operation is to be performed, said memory bank control signal generating circuit generating memory bank control signals to enable a refresh operation with respect to the identified memory bank.

12. A method for operating a memory controller for use in a digital computer system having a bus, the memory controller for controlling a memory including a plurality of memory banks, each memory bank including a plurality of storage locations, said memory system for initiating a memory access operation in connection with a storage location in a selected bank, said method comprising the steps of:

A. receiving memory access requests over the bus and performing a memory access operation in connection with a storage location in response thereto;

B. generating a timing signal to indicate an end of each of a succession of predetermined time intervals;

C. selecting a memory bank following the generation of the timing signal concurrent with the performance of a memory access operation to a memory bank, the selected memory bank being other than the memory bank with which the memory access operation is being performed;

D. initiating a concurrent refresh operation in connection with the selected memory bank (following the generation of the timing signal concurrent with the performance of a memory access operation, the concurrent refresh operation being initiated in connection with a memory bank other than a memory bank with which the memory access operation is being performed,) and maintaining concurrent refresh status information indicating refresh status of each said memory bank; and

E. determining in response to a timing signal and the concurrent refresh status information the refresh status of each said memory bank and initiating an urgent refresh operation in response to generation of the timing signal in connection with a memory bank which was not refreshed by concurrent refresh operations during the preceding timing interval, and disabling said memory access operations during said urgent refresh operation, except for

performing said refresh operation."

IV. The appellant argued in the statement of grounds that the present invention concerned a memory controller for **a plurality** of memory banks, not just two memory parts as disclosed in document D1. During access to a first memory bank, a concurrent refresh control circuit initiated a refresh operation in connection with a **selected** second memory bank. Thus, during concurrent refreshing, only two memory banks were operated upon despite a memory refresh controller being responsible for multiple memory banks. In order to apply the memory system of D1 to a large number of memory banks, the memory banks would first have to be organised into pairs, each pair having a refresh timing circuit, two control circuits and counters. In contrast thereto the present invention was much simpler and involved therefore an inventive step.

V. In a communication annexed to the summons to attend oral proceedings, the Board informed the appellant that although differences between the subject-matter of the present application and the cited prior art could be seen from the explanation in the grounds of appeal, the claims filed therewith did not appear to define inventive differences with sufficient clarity.

Regarding claim 1 of the main request it appeared that in the first paragraph between the words "plurality of" and "storage" the words "memory banks (15A,N), each memory bank including a plurality of" had been left out and that in claim 1, fifth paragraph (paragraph Bii) the passage "refresh control circuit initiating a refresh operation in connection with a memory bank" had been shrunk to "rebank". Since two memory parts I and

II described in document D1 involved more than one bank, document D1 concerned also a plurality of banks. It was doubtful whether the subject-matter of claim 1 (main request) was new, or involved an inventive step, having regard to D1.

Similar objections were made with respect to claim 12 of the main request and claims 1 and 12 of the auxiliary request.

VI. In a letter dated 8 September 2000 the representatives informed the Board that the applicant had instructed them not to attend the oral proceedings on 10 October 2000. The oral proceedings were held on 10 October 2000 in the absence of the appellant. It was noted that no attempt had been made to answer the outstanding objections.

Reasons for the Decision

1. The appeal is admissible.

2. In the communication of the Technical Board of Appeal dated 11 May 2000 the appellant was informed about numerous deficiencies in the independent claims 1 and 12 of the main and auxiliary requests (see paragraph V above), such that claims 1 and 12 of the main and auxiliary request do not clearly define the matter for which protection is sought as required in Article 84 EPC. These claims are therefore not allowable. Attention is drawn to Article 113(2) EPC and decision T 32/82 (OJ 1984, 354), according to which a Board of Appeal has no authority to order the grant of a patent containing claims which are different from those

submitted by the applicant.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Hörnell W. J. L. Wheeler