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D E C I S I O N
of 16 November 1999

Case Number: T 0299/98 - 3.5.1

Application Number: 89313671.3

Publication Number: 0377330

IPC: G05B 19/04

Language of the proceedings: EN

Title of invention:

Multiple material processings system start-up

Applicant/Patentee:

PITNEY BOWES INC.

Opponent:

- (01) Société Secap
(02) Francotyp-Postalia GmbH

Headword:

-

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step (no)"

Decisions cited:

-

Catchword:



Case Number: T 0299/98 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 16 November 1999

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Decision under appeal: Interlocutory decision of the Opposition Division
of the European Patent Office posted
27 January 1998 concerning maintenance of

Composition of the Board:

Chairman: P. K. J. van den Berg

Members: R. S. Wibergh

S. C. Perryman

Summary of Facts and Submissions

I. The present appeals are against the decision of the Opposition Division to maintain European patent No. 0 377 330 in amended form. The appeals have been filed by the Patentee and by Opponent 1. Opponent 2 is a party to the proceedings as of right.

II. Opponent 1 had opposed the patent on the grounds that the invention was not new or did not involve an inventive step having regard to - among others - the documents

O1D1: Datapro Research Corp. 1976 "IBM Synchronous Data Link Control (SDLC)", pages manually numbered 1 to 6,

O1D2: Manual "IBM Synchronous Data Link Control General Information, 1974, pages 3-1 to 3-13, and

O1D3: US-A-4 562 535.

III. Opponent 2 had opposed the patent on the ground that the invention did not involve an inventive step. In particular, the following documents were cited:

O2D2: DE-A-3 347 357

O2D7: DE-A-3 328 834

O2D8: EP-A-0 208 998.

IV. The Opposition Division held that the subject-matter of claim 1 according to the then main request was not inventive over prior art mainly cited by opponent 2. It was also decided that the invention was new with respect to the prior art cited by opponent 1, in particular O1D1 and O1D2, but the question of inventive step in respect of these documents was not discussed. The subject-matter of claim 1 of the then auxiliary request was regarded as patentable.

V. The Patentee and Opponent 1 lodged appeals against this decision. Opponent 1 filed a new document together with the grounds of appeal,

O1D4: EP-A-0 192 795.

O1D4 was said to demonstrate the obviousness of the invention as claimed in the patent in the maintained version.

VI. On 27 October 1998 the Patentee filed new claims according to a main request (Claim Set A) and an auxiliary request (Claim Set B).

Claim 1 of the *main request* read as follows (omitting the reference signs):

"A material processing system comprising a plurality of peripheral modules and a base module, said base module including a central processor, each of said peripheral modules including a peripheral processor, and

- a serial data link inter-connecting said processors in a serial manner to form a

communication loop, said central processor including means for providing a system command signal along said serial link to the first of said peripheral module processors,

- each said peripheral processor including means responsive to said system command signal for adding thereto a tag, said tag including data representative of the address and configuration of said processor and for passing said system command signal along said serial data link to the next successive module processor, the system command signal thus passing from module to module around the loop accumulating the tags from all respective peripheral processors, until the last of the peripheral processors passes said system command signal and tags appended thereto to said base module central processor, and
- said base module central processor including storage means for storing the address and designation data of each said module, and being operable to store the address and designation data of each module in response to receipt of the system command signal and respective tags."

VII. Claim 1 according to the *auxiliary request* added the feature that the system comprises a multi-drop data bus which functions to provide direct bidirectional communication between the base module central processor and each of the peripheral processors.

VIII. On 12 October 1999 the Patentee filed a prior art document,

P1: US-A-3 633 166.

- IX. Oral proceedings before the Board were held on 16 November 1999.
- X. The Patentee argued that the invention as defined in claim 1 as granted was new and inventive with respect to all cited prior art. P1 served to explain the somewhat obscure teaching of O1D1 and O1D2 and highlighted the main difference between the invention and this prior art. The invention according to the auxiliary request was even more clearly inventive since it provided a synergetic effect. As to O1D4, this document had been filed late and should not be allowed into the proceedings.
- XI. Opponent 1 argued that the invention according to the main request was not new with respect to O1D1 and O1D2, two documents which should be regarded together since they described the same system. Furthermore, if the invention were new it would still lack an inventive step in view of a combination with the further document O1D3.

The addition of a feature in accordance with the auxiliary request involved no inventive step in view of the skilled person's general knowledge. Furthermore, the additional feature was known from O1D4.

- XII. Opponent 2 argued that the invention was obvious in view of O2D7 or a combination of O2D7 and O2D2. O2D8 was regarded as less relevant than O1D1 or O1D2.
- XIII. The Patentee requested that the decision under appeal

be set aside, and as main request that the patent be maintained on the basis of Claim Set A filed on 27 October 1998, and as auxiliary request that the patent be maintained on the basis of Claim Set B filed on 27 October 1998 and that document O1D4 not be admitted into the proceedings or if document O1D4 be admitted into the proceedings that the matter be remitted to the first instance for further prosecution with an apportionment of costs in his favour.

XIV. Opponent 1 requested that the decision under appeal be set aside and that the European patent be revoked.

XV. Opponent 2 requested that the appeal of the Patentee be dismissed.

Reasons for the Decision

The Patentee's main request

1. *The invention*

The invention is a "material processing system" mainly characterised by features relating to a serial data link combining a base module with a plurality of peripheral modules. The serial link is in the form of a loop. The base sends a command around the loop to which the peripherals respond. They do this in the form of a "tag" which is added to the command signal, and the command is returned to the base with all the tags appended. The tags contain information about the address and configuration of the peripherals. The

procedure can therefore be used in particular to inform the base automatically on power-up what peripherals are on the loop, their number, respective addresses and capabilities. As said in column 18 of the patent, this is a simplification compared with previous systems which required a configuration PROM to be installed.

2. *Novelty*

2.1 Opponent 1 relies mainly on the two documents O1D1 and O1D2 which describe the IBM "Synchronous Data Link Control" (SDLC) system. This system comprises a data link, which may be formed as a loop, connecting a base module ("primary station") to peripheral modules ("secondary stations"). There is a poll command, referred to as NSP in O1D1 and as ORP in O1D2, to which the peripherals respond. As can be seen from page 3-13 of O1D2, the responses (consisting of a request for online status: ROL) can be regarded as tagged to the GA (Go Ahead) command issued by the base module immediately after the ORP command. Each response contains the address of the peripheral in question. The base station then uses the address information to change the status of each individual peripheral from the Normal Disconnect Mode to the Normal Response Mode.

2.2 Opponent 1 has submitted that the invention is not new with respect to the IBM system. This the Patentee has denied. According to the Patentee, although information may perhaps be tagged onto the GA command, this information does not comprise data about the *configuration* of the peripheral. Furthermore, in the prior art peripherals would not *have* to respond to the poll command.

- 2.3 The Board finds that the prior art does in fact not disclose that configuration data are tagged to the command signal. According to O1D2, page 2, polled secondary stations respond either with a request for online status (ROL) or for initialisation (RQI). These predetermined responses have nothing to do with the configuration of the processor in the peripheral. They can only indicate the current state of the peripheral.
- 2.4 On the other hand, the Board does not interpret O1D2 and O1D1 in the way that the response to the poll command is always optional (in spite of the name of this command: ORP, Optional Response Poll). According to O1D1, page 2, a secondary station in the so-called Normal Disconnect Mode (NDM) responds to polls with a request to be put on line or to be initialised, and ignores other commands. This, in the Board's view, can only be understood in the way that the station is *obliged* to respond to a poll when it is in the NDM mode. Furthermore, according to the passage bridging pages 4 and 5, the poll command either invites a response or *requires* it, depending on the value of a certain command bit.

To support his view the Patentee has referred to a number of passages in the documents, such as O1D2 page 3-3 ("response to the P-bit is *optional*") and page 3-5 ("the first down-loop secondary station with the authority and *need* to transmit... starts to transmit"; "the next down-loop secondary station has the *opportunity* to transmit"). These examples do show that response to the poll command may be optional. But they do not seem to prove that the response is optional under all circumstances, and in particular when the

secondary stations are in the NDM mode.

In this context the Patentee has also cited document P1. P1 shows a loop configuration and command structure which appears to be consistent with SDLC and where the response to the poll command indeed appears to be optional. There is however no explicit reference to SDLC in P1, and even if there had been one, the document contains no listing of the available commands, let alone one which would contradict the teaching of O1D1 and O1D2. The crucial question whether SDLC poll commands are *always* optional is therefore not answered by this document.

It follows that O1D1 is regarded as disclosing the feature that tags from *all* peripherals are accumulated. Thus this characteristic in claim 1 is not new.

2.5 The Board furthermore notes that the invention as claimed is a *material processing* system. O1D1 and O1D2 describe the general principles of the link in terms of primary and secondary stations. These principles - as usual in this technical domain - will be "independent of application and terminal type" (O1D1, page 1). The only mentioned use of the link is for a teller terminal system for financial institutions (O1D1, page 1). Although it is very likely that such a system will involve some material processing - simply printing records might arguably be regarded as a kind of paper processing - no such feature is actually disclosed.

2.6 The invention is thus new since neither O1D1 nor O1D2 discloses

- (a) that the tags contain data about the configuration of the peripheral, and
- (b) that the link control is applied to a material processing system.

3. *Inventive step*

- 3.1 Starting out from the SDLC system as it has been described in O1D1 and O1D2, the main problem to be solved is the one indicated in the opposed patent, column 17, viz. to provide automatic configuration of equipment without the need for a configuration PROM.
- 3.2 The Patentee has not contended that the detection of this problem has inventive merit, and indeed the Board finds that it has not. Although configuration data is not an issue in O1D1 and O1D2 it is clear that the primary station will normally have to know the capabilities of the secondary stations. As new secondary stations are added to the link, the primary station must be informed of their configuration. The most straight-forward way to achieve this would perhaps be to let an operator input the data, but an automatic configuration process would obviously be preferable.
- 3.3 This problem has been addressed and solved in O1D3. This document relates to a self-configuring processor system. In columns 12 and 13 it is said that the purpose of this system is to make address decode PROMs unnecessary by establishing module addresses automatically on power-up. At this time every module stores data about itself, including a list of the functions it can perform, in a central memory. The

Board is of the opinion that such a list can be termed configuration data.

3.4 Because of the mentioned advantages, the skilled person would want to add this feature to the SDLC system. The next question is therefore whether the combination would have caused technical difficulties which required inventive skill to overcome.

3.5 At first sight, the combination appears simple enough: it would suffice to add configuration data to the address data provided by each secondary unit when it is polled in the NDM mode (ie in particular on power-up).

The Patentee, however, points out that there are considerable differences between the link described in 01D3 and the SDLC link. In 01D3 there is in particular a bus rather than a loop, there is no primary station, no accumulation of tags, and all the modules contend for access to the bus.

3.6 While acknowledging these differences, the Board nevertheless finds the combination straight forward. The configuration problem is not restricted to a certain link architecture. Therefore the skilled person would not pay attention to irrelevant differences but would go straight to the features which actually serve to solve his problem and see if and how they could be incorporated in the link he is concerned with. According to 01D3 configuration data are transferred to a central memory. It is clearly not decisive *how* the data are transported and therefore the skilled person would not be disturbed by the different link structure in 01D3. Nor does it matter whether the central memory

is associated with a primary station or not, as long as the configuration data can be made available to the system as a whole.

3.7 Therefore difference (a) at point 2.6 above, ie the feature that the tags contain data also about the configuration of the peripheral, is regarded as obvious in view of 01D1/01D2 taken together with 01D3.

3.8 As to the difference (b), the incorporation of the SDLC link in a material processing system was also obvious. A "material processing system" - a general term - is understood as any system which is not a pure data processing system. The skilled man would not see the secondary stations in 01D1 and 01D2 as modules intended exclusively for data processing, "material processing" applications being generally known. One such example is incidentally given in 01D3 (column 2, line 15), viz. the control of industrial robots.

Furthermore, as already noted at point 2.5 above, the border line between data processing systems and material processing systems is not always easy to draw.

4. For these reasons the subject-matter of claim 1 does not involve an inventive step.

The Patentee's auxiliary request

5. The system according to the auxiliary request comprises additionally a multi-drop data bus. This bus provides direct bidirectional communication between the base

module and each of the peripheral processors. The Patentee has explained that the task of the multi-drop bus is to ensure high-speed transmission of data.

6. The Board first notes that the Patentee does not claim to have invented the multi-drop bus as such. This kind of bus was known and thus also its properties, such as its capacity for high-speed data transfer. It was furthermore known that serial loops, such as the one described in O1D1 and O1D2, are in general relatively slow. The addition of a multi-drop bus to the known loop structure could therefore be seen as an obvious solution to a problem which was bound to manifest itself sooner or later, namely the need to transfer (large amounts of) data at high speed between the primary station and the secondary stations.
7. The Patentee has submitted that a synergistic relationship exists between the serial loop and the multi-drop bus. The loop provides the base station with the addresses of the peripheral modules and these addresses are used also for the bus. Without the loop the base module would not have this information.

Opponent 1 denies that there is any kind of synergy. The loop provides module configuration data and the bus provides a high-speed connection. The features are juxtaposed. Even if the module addresses used by the bus have been communicated to the base station over the loop this is merely an example of one device of a system using the output of another device, similar to the "machine for producing sausages" mentioned in the Guidelines C-IV-annex, 2.1.

8. The Board takes the view that the existence of a synergistic effect has not been convincingly demonstrated. The word synergy implies that (known) means cooperate to achieve a result which is more than the sum of the capabilities of each individual means. Here this is not the case. It is prior art that the module addresses are transmitted over the loop, and it is also prior art that a multi-drop bus has to use some kind of addresses. The juxtaposition of the features indeed leads to the invention without any further effect being obtained: the loop provides the addresses and the bus simply uses them in the normal way. It should perhaps also be noted that claim 1 contains no details about the addressing method used. In fact, the bus addressing is only implied.

9. It follows that also the Patentee's auxiliary request is refused. His further requests for remittal of the case to the Opposition Division for assessment of O1D4 - a document the Board has not found necessary to discuss in the present decision - and for apportionment of costs need therefore not be considered.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The patent is revoked.

The Registrar:

The Chairman:

M. Kiehl

P. K. J. van den Berg