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D E C I S I O N
of 22 February 2000

Case Number: T 0296/98 - 3.5.2

Application Number: 96103503.7

Publication Number: 0731563

IPC: H03K 19/08

Language of the proceedings: EN

Title of invention:
A BiCMOS logic gate

Applicant:
NEC CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 111(2)

Keyword:
"Novelty - yes"
"Remittal to first instance"

Decisions cited:
-

Catchword:
-

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Case Number: T 0296/98 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 22 February 2000

Appellant: NEC CORPORATION
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 5 November 1997 refusing European patent application No. 96 103 503.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: F. Edlinger
B. J. Schachenmann

Summary of Facts and Submissions

I. The applicant filed this appeal against the decision of the examining division to refuse the European patent application No. 96 103 503.7. The reason given for the refusal was that the subject-matter of claims 1 and 4 as originally filed lacked novelty with respect to the prior art disclosed in EP-A-0 606 766 (D1).

II. The contested decision is essentially based on the finding that the "circuit details" of Figure 1 of the present application were anticipated by D1, in particular Figure 6. Differences in the "particular dimensioning" referred to by the applicant were considered as irrelevant because the claims did not contain corresponding features. Dependent claims 2, 3 and 5 were held not to contribute anything patentable because the "circuit details" added by these claims were included in Figure 1 of the present application which was fully anticipated by the prior art disclosed in D1.

III. With letter dated 24 January 2000 filed in response to a communication issued by the board, the appellant filed amended claims 1 to 4 (headed "main request"), claim 1 of which was amended during oral proceedings held on 22 February 2000.

IV. Claim 1 now reads as follows:

"A BiCMOS logic gate comprising:
a pair of MOS transistors (6, 7) having their sources coupled with each other and having their gates supplied with respective complementary logic input signals;

a constant current source connected between a connection of said sources of said MOS transistors (6, 7) and a first terminal (VEE) of a power supply, said constant current source including a bipolar transistor (5) with a base controlled by a reference voltage (VCS);
a pair of load elements (3, 4) each connected between the drain of a respective one of said MOS transistors (6, 7) and a second terminal (GND) of said power supply, and wherein the voltage differences generated by said pair of load elements (3, 4) are output as respective complementary logic output signals, and
a drain current intensity of the MOS transistor (6, 7), which is in an ON-status, is determined by a current intensity of said constant current source;

characterized in that

circuit constants of the BiCMOS logic gate, including current intensity of said constant current source, said pair of said MOS transistors (6, 7) and resistances of said load elements (3, 4) are designed so that an input dynamic range is more than 1/2 of an output dynamic range and not more than the output dynamic range."

Claims 2 to 4 are dependent on claim 1.

V. The appellant argued essentially as follows:

The contested decision already admitted that subject-matter comprising the particular dimensioning of the circuit as now specified was new over the cited prior art. D1 merely disclosed CMOS to ECL level converters where the input dynamic range was higher than the

output dynamic range as could be seen from Figure 7B of D1. The subject-matter of claim 1 was thus novel.

In the oral proceedings before the board, the appellant declared that he did not wish to comment on the significance of the distinguishing features since the only ground for refusal, lack of novelty, was overcome by the amended claims.

VI. The appellant requested that the decision under appeal be set aside and that the case be remitted to the first instance for further prosecution of the application on the basis of claim 1 as filed in the oral proceedings and claims 2 to 4 as filed with the letter dated 24 January 2000.

Reasons for the Decision

1. The appeal is admissible.

2. The question to be answered in this appeal is whether the subject-matter of claims 1 to 4 is new with respect to the state of the art disclosed in D1. However, the claims have been amended in the appeal proceedings, and it has to be first examined whether the amendments are allowable and whether the claims are sufficiently clear for the question of novelty to be decided.

3. Claim 1 has been amended by adding features to claim 1 as filed and by improving its language. The additional features are disclosed in the application as filed on page 12, lines 4 to 8, in combination with Figure 1 (the last feature of the first part of claim 1), in

claims 5 and 16 and on page 8, lines 17 to 21, in combination with Figure 3 (characterising portion of claim 1). Dependent claims 2 to 4 are respectively based on claims 5, 2 and 3 as filed. Claims 1 to 4 therefore do not infringe Article 123 (2) EPC.

4. The term "dynamic range", in its general meaning in different electrotechnical fields, usually refers to a ratio or a difference of maximum and minimum signal levels, often expressed in decibels. The terms "input dynamic range" and "output dynamic range" used in the characterising portion of claim 1 are to be seen in the context of the complementary logic input and output signals of the BiCMOS logic gate. On a context-related construction of these terms as used in the present application, they refer to an input dynamic range which is determined by logic high and low input signal levels capable of causing a corresponding change in the output signal levels determining said output dynamic range. In other words, these terms refer to the logic swing at an output of the BiCMOS gate as claimed (see also claim 2) when the logic input signal changes between acceptable logic high and low levels within the specified input dynamic range. Claim 1 specifies a relationship between the input dynamic range and the corresponding output dynamic range. The description of the application as filed (page 4, lines 11 to 15, in combination with Figure 14; page 14, lines 11 to 24, and page 15, lines 14 to 20, in combination with Figure 3) explains that the logic gate of the present application, due to the fact that MOS transistors have a smaller mutual conductance compared with bipolar transistors, results in a smaller difference between the input dynamic range and the output dynamic range, as compared to the known

ECL gate shown in Figure 12 of the present application.

5. These passages all refer to embodiments where the dynamic range is expressed as a voltage difference (in mV). However, it is noted that in the case of the disclosed example of input voltage levels (0.9 V and 1.5 V; see page 19, lines 5 to 7) and if output voltage levels are the same as the input voltage levels ("have the same voltage swing width", see claim 2; "voltage gain ... not smaller than 1", page 15, lines 14 to 16), a comparison of a ratio of (typical) input voltage levels with a ratio of (typical) output voltage levels could also make technical sense. This does not however influence the decision on novelty (see point 6 below).

6. D1 (page 1, lines 10 to 17; Table 2; Figures 6 and 7B) discloses a BiCMOS logic gate comprising the features of the first part of present claim 1 as was acknowledged by the appellant. These circuits serve to convert CMOS input signals to ECL or CML output signals. The input dynamic range of these gates with CMOS levels at the inputs (approximately 3 V or 0 V) is therefore greater than the output dynamic range (ECL levels of 800 mV or 400 mV) independently of whether the dynamic ranges are taken as voltage differences or as voltage ratios. Claim 1 of the present application, however, specifies that the input dynamic range is "not more than the output dynamic range" which excludes converters of this type.

7. The subject-matter of claim 1 shall thus be considered to be new (Articles 54(1) and (2) EPC) with respect to the state of the art disclosed in D1. Claims 2 to 4 are dependent on claim 1 and shall thus also be considered

to be new with respect to the state of the art disclosed in D1.

8. The board wishes to emphasize that the department of first instance shall be bound only by the *ratio decidendi* (Article 111(2) EPC) in so far as it has been decided that the subject-matter of the present claims 1 to 4 is novel over D1. Other questions, in particular whether the claimed subject-matter involves an inventive step have been left for the first instance to decide upon. Furthermore, although the board considers the claims to be clear enough to enable it to establish novelty, it may be that further amendments may be necessary to satisfy all the requirements of the Convention, including the specification of all the essential features for solving the problem underlying the present application.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance for further prosecution of the application on the basis of claim 1 as filed in the oral proceedings and claims 2 to 4 as filed with the letter dated 24 January 2000.

The Registrar: The Chairman:

M. Kiehl W. J. L. Wheeler