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D E C I S I O N
of 12 March 2002

Case Number: T 0220/98 - 3.4.3

Application Number: 91105165.4

Publication Number: 0450558

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:
Semiconductor device and method of manufacturing the same

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
Liquid phase deposition/TOSHIBA

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0220/98 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 12 March 2002

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 13 October 1997 refusing European patent application No. 91 105 165.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 91 105 165.4 was refused in a decision of the examining division dated 13 October 1997. The ground for the refusal was that the application did not meet the requirements of inventive step having regard to the prior art documents

D3: Proceedings 1987 Fall Meeting of the Materials Research Society, Boston, MA, 30 November to 5 December 1987, T. Goda et al." "Physical and Chemical Properties of Silicon Dioxide Film Deposited by New Process"; and

D4: EP-A-0 285 245.

Furthermore, it was held in the decision that claims 20 and 21 of the applicant's requests relating to a semiconductor device were not clear.

Following prior art document was also cited in the examination proceedings:

D1: EP-A-0 223 637.

II. The reasoning in the decision of the examining division in respect of the issue of inventive step, can be summarized as follows:

(a) Document D4 discloses a conventional method of forming a semiconductor device where an inorganic oxide layer is deposited on a plurality of wires, followed by a step of flattening the inorganic oxide layer. The claimed method differs from the known method in that the oxide layer on the

plurality of wires is formed by precipitation from a supersaturated solution of the oxide in hydrofluoric acid (in the following referred to as the LPD method).

(b) The problem addressed by the application in suit was to form an inorganic oxide layer at a lower temperature than that used in the conventional method.

(c) Document D3 discloses a method of depositing silicon oxide using the LPD method on a silicon substrate for the purpose of providing insulation, passivation and isolation in electronic devices. Since the deposition takes place at room temperature, the skilled person would contemplate in advance the advantages of this method so as to avoid problems of the conventional method where the metal wires are exposed to high temperatures during the deposition of the oxide layer. Thus, the replacement of the conventional deposition method by LPD is considered obvious.

III. The appellant (applicant) lodged an appeal on 15 December 1997, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 20 February 1998 together with new claims according to a main request.

IV. In response to a communication accompanying the summons to oral proceedings, the appellant filed on 12 February 2002 four sets of claims according to first to fourth auxiliary requests, respectively.

V. At the oral proceedings held on 12 March 2002, the

appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of one of the following requests:

Main Request:

Claims 1 to 7 according to the Main Request as filed on 20 February 1998 with the statement of the grounds of appeal;

or on the basis of the **First Auxiliary Request** to **Fourth Auxiliary Request** filed on 12 February 2002.

VI. Claim 1 according to the appellant's main request reads as follows:

"1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a first insulative layer (2) on a semiconductor substrate (1);

forming a plurality of wires (11A, 11B) on said first insulative layer, said plurality of wires being polysilicon or acid-resistant metal which comprises one of tungsten, nickel and molybdenum; and

forming a second layer (3) completely filling at least a gap between said plurality of wires, said layer (3) comprising one of silicon oxide, tungsten oxide and tantalum oxide obtained by precipitation from a supersaturated solution of the oxide in hydrofluoric acid."

Claim 2 is a further independent method claim and claims 5 and 6 are independent claims both directed to a semiconductor device.

VII. Claim 1 according to the appellant's first auxiliary request differs from claim 1 according to the main request in that (i) the second layer (3) is further specified to comprise "an inorganic oxide"; and (ii) the method further comprises a final step of

> "etching back said second layer (3), thereby flattening the surface of the inorganic oxide."

Claims 2, 4, and 5 are further independent claims.

VIII. Claim 1 according to the appellant's second auxiliary request differs from claim 1 according to the main request in that (iii) the materials of the plurality of wires (11A, 11B) are restricted to polysilicon or tungsten.

Claims 2, 5, and 6 are further independent claims.

IX. Claim 1 according to the appellant's third auxiliary request differs from claim 1 according to the main request in that it includes the features (i) to (iii) above, and (iv) further includes the following final step:

> "optionally, forming a second insulative layer (5) on the layer (3), and forming a further plurality of wires on the layer (3) or on the optional second insulative layer (5) on the layer (3), when present."

Claims 2, 4, and 5 are further independent claims.

X. Claim 1 according to the appellant's fourth auxiliary request reads as follows:

"1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a first insulative layer (2) on a semiconductor substrate (1);

forming a plurality of wires (11A, 11B) on said first insulative layer, said plurality of wires being polysilicon or tungsten;

forming a layer (3) completely filling at least a gap between said plurality of wires, said layer (3) comprising an inorganic oxide and comprising one of silicon oxide, tungsten oxide and tantalum oxide obtained by precipitation from a supersaturated solution of the oxide in hydrofluoric acid;

etching back said layer (3), thereby flattening the surface of the inorganic oxide;

forming a second insulative layer (5) on said layer (3); and

forming a further plurality of wires on the second insulative layer (5)".

Claims 2, 4, and 5 are further independent claims. They are not relevant for the present decision.

XI. The appellant presented essentially the following arguments in support of inventive step:

(a) In the decision under appeal, it was stated that the problem addressed by the present invention relates to forming an inorganic oxide layer on a conductor device at a lower temperature than that used in the conventional methods. The conventional CVD methods for deposition silicon oxide as described in document D4 operate at a temperature of about 400 °C which is low enough for not causing major damage to the semiconductor device. Therefore, the skilled person would not consider the deposition temperature to be a problem. The present invention addresses the problem of avoiding the formation of voids, known in the art as "nests", in an inorganic oxide layer provided between two adjacent wires. This problem arises in particular in cases of silicon oxide grown by CVD (cf. the application as published, column 2, lines 48 to 56). However the problem of formation of voids or nests is not disclosed in the prior art.

(b) Document D3 cannot be relied on as a secondary prior art reference, since the distribution of document D3 was very restricted. Therefore, since document D3 would not have been available to the skilled person as a secondary reference, it would not be realistic to expect that the skilled person would be in a position to even contemplate the combination of the teaching of the documents D3 and D4.

(c) Nevertheless, even if one would contemplate a

combination of the documents D3 and D4, there is no disclosure or suggestion to use the specially selected materials defined in claim 1 to form the conductive wires, or the specially selected materials in claim 2 to cover the conductive wires.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. It follows from the wording of claim 1 of the fourth auxiliary request that the claim incorporates the entire subject matter of claim 1 of each of the preceding requests. In the following, therefore, the issue of inventive step only of claim 1 of the fourth auxiliary request is considered, the reasoning in the discussion being applicable to claim 1 of all the preceding requests. Also, since the subject matter of claim 1 is not patentable for lack of inventive step for the reasons given below, the Board does not consider it necessary to consider other requirements of the Convention such as the requirements of Articles 84 and 54 EPC in respect of the independent device claims of the appellant's requests.

3. *Inventive step - Fourth Auxiliary Request*

3.1 The application in suit relates to integrated circuits and methods of producing such integrated circuits, and, in particular, is concerned with forming insulating layers, the so-called interlayer insulative layers, for insulating wiring levels from each other. A

conventional method referred to in the application in conjunction with Figure 2 comprises the steps of forming a first insulating layer 2 on a semiconductor substrate, forming a plurality of wires 11A, 11B on the first insulating layer, and depositing an inorganic oxide layer 4 using plasma enhanced chemical vapor deposition (PECVD) (cf. the application as published, column 2, lines 20 to 47; Figure 2). After the oxide layer 4 has been formed, it is planarized using a conventional etch-back technique. A second insulative layer 5 is formed on the planarized oxide layer 4, followed by the formation of a second plurality of wires 21A, 21B on the second insulative layer 5.

The same conventional method is also described in document D4 (cf. page 2, line 54 to page 3, line 15).

3.2 The method of claim 1 differs from the above prior art method in that (i) the oxide layer formed on the plurality of wires is obtained by precipitation from a supersaturated solution of the oxide in hydrofluoric acid; and (ii) the wires are made of polysilicon or tungsten, whereas in the prior art method, aluminum is used.

3.3 The technical problems addressed by the application in suit are that (i) the oxide layer 4 formed by PECVD had a tendency to form voids, sometimes referred to as "nests", in the gaps between two adjacent wires; and (ii) the high temperatures required for producing oxide layers using thermal oxidation is likely to damage the wires (cf. application as published, column 2, lines 48 to 56 and column 3, lines 17 to 27). It is furthermore mentioned in the application in suit, that an oxide layer used as an interlayer insulating

layer of an integrated circuit must meet several criteria such as high quality, absence of pin holes, high withstand voltage, and low moisture absorption property, in order to ensure proper functioning of the semiconductor device (cf. column 1, lines 19 to 31 and column 3, lines 21 to 27).

3.3.1 In the decision under appeal, only the problem of high deposition temperature (problem (ii)) was considered. As the appellant convincingly argued, however, a conventional CVD method of deposition silicon oxide is carried out at about 400 °C which is normally not considered as being too high (cf. item XI(a) above). The problem of high temperatures mentioned in the application in suit referred to a different prior art method where the oxide layer 4 was formed using thermal oxidation (cf. column 3, lines 11 to 20).

Although the problem of avoiding voids in the oxide layer is mentioned in the application in suit, it is also stressed that several other factors, such as having few pinholes, a high withstand voltage, and a flat surface must be considered as well. Therefore, the technical problem addressed by the application in suit relates to finding an alternative method of forming an inorganic oxide layer which meets all the requirements of an interlayer insulating film, such as avoiding voids.

3.4 The appellant argued that the technical problem of avoiding voids or nests in an oxide layer had not been addressed in the prior art documents (cf. item XI(a) above). The Board however cannot follow this argument for the following reasons:

Document D1 discusses the problem of forming an oxide film having a uniform thickness on high density interconnection wires (cf. column 1, lines 10 to 63). In particular, using a conventional method of CVD, the deposited oxide film develops cusps at the upper corner of the wire and has reduced thickness at the lower corner resulting in a void in the oxide film.

Thus, the above citation shows that the task of completely filling a gap between two adjacent wires of an integrated circuit with an oxide layer was known to be difficult, and that oxide layers deposited using CVD techniques, in particular, had problems in this respect. The Board therefore concludes that although the problem of avoiding the formation of voids or nests is not explicitly mentioned in document D1, the problem of completely filling a gap between the wires with an oxide layer was well-known in the art at the priority date of the application in suit.

3.5 Document D3 is a manuscript of a paper presented at the 1987 Fall Meeting of the Materials Research Society. It was subsequently published in 1988 in facsimile form in a conference proceedings book (ISBN 0-931837-73-1), ie well before the priority date of the application in suit. Thus, contrary to the doubts raised by the appellant, document D3 was available to the public before the priority date of the application in suit (cf. item XI(b) above).

3.6 Document D3 describes the deposition of silicon oxide on silicon substrates by precipitation from a supersaturated solution of the oxide in hydrofluoric acid (in the following referred to as LPD process (Liquid Phase Deposition)). The deposited oxide layers

have a good "step coverage", ie the ability to cover steps on a surface (cf. abstract). Furthermore, the LPD technique for forming oxide layer is suggested to be useful for insulation, passivation and isolation in electronic devices (cf. "Introduction", first paragraph).

3.7 A skilled person faced with the task of finding an alternative to the CVD method of forming the oxide layer 4 in the prior art method would in the Board's opinion consider document D3, since it reported to have a good step coverage which is a prerequisite for covering wires on an integrated circuit. Moreover, since the LPD deposition method of document D3 involves dipping the silicon substrate in a saturated solution of the oxide in hydrofluoric acid, it is evident to the skilled person that such a method would have great potential of being able to form an oxide layer without voids in the regions between two adjacent wires.

The Board is furthermore of the opinion that the skilled person would be aware of the corrosive properties of hydrofluoric acid, and that the features to be covered by the oxide layer, ie the wires and the underlying first insulating layer, thus have to be made of materials withstanding the exposure to hydrofluoric acid. Since both polysilicon and tungsten are well-known alternatives to aluminum as material for wiring layers in integrated circuits, and since their chemical properties are in general known, the skilled person would try these materials as a matter of routine (cf. item XI(c) above).

3.8 Therefore, in the Board's judgement, the subject matter of claim 1 according to the fourth auxiliary request

does not involve an inventive step within the meaning of Article 56 EPC.

4. Since claim 1 according to all the requests do not meet the requirements of inventive step (cf. item 2. above), these requests are not allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla