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D E C I S I O N
of 5 February 2002

Case Number: T 0195/98 - 3.4.3

Application Number: 90104813.2

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IPC: H01L 27/06

Language of the proceedings: EN

Title of invention:

Semiconductor structure for processing and storing of
information

Applicant:

KABUSHIKI KAISHA TOSHIBA

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 54 and 56

Keyword:

"Main request: Novelty (no)"

"Auxiliary request: Inventive step (no) (obvious alternative
arrangement)"

Decisions cited:

-

Headnote/Catchword:

-



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Boards of Appeal

Chambres de recours

Case Number: T 0195/98 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 5 February 2002

Appellant: KABUSHIKI KAISHA TOSHIBA
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210-8572 (JP)

Representative: Lehn, Werner, Dipl.-Ing.
Hoffmann Eitle
Patent- und Rechtsanwälte
Postfach 81 04 20
D-81904 München (DE)

Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 13 October 1997
refusing European patent application
No. 90 104 813.2 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. B. Tardo-Dino

Summary of Facts and Submissions

I. The European patent application No 90 104 813.2 (Publication No. 0 387 834) was refused by a decision of the examining division dated 13 October 1997 on the ground that claim 1 of the main and the auxiliary request lacked an inventive step having regard to the prior art document

D5: US-A-4 424 579.

II. Claim 1 of the main request forming the basis of the decision of the examining division reads as follows:

"1. A semiconductor device having a first functional block (202) for processing data for logical operation and data control and a second functional block (206, 302) for previously storing information required for the data processing both on a semiconductor substrate (100) in the form of a silicon layer, wherein:

the first functional block (202) is formed directly on the semiconductor substrate (100);

the second functional block (206, 302) includes a memory cell array (302) having a plurality of memory cells, and a functional element section (206) at least for reading data from said memory cell array;

said functional element section (206) is formed directly on the semiconductor substrate;

said silicon layer (100) is included as part of the first functional block (202) and the functional element section (206) of the second functional block (206, 302);

a first insulating film (110) is formed on said first functional block and on said functional element section;

said memory cell array (302) is formed on said first insulating film (110) and comprises a first arrangement of conductive wires (112) extending in an X-direction, and a second arrangement of conductive wires (115) extending in an Y-direction, which first and second arrangements have a second insulating film (113) interposed therebetween and the X-direction and Y-direction conductive wires of which are three-dimensionally intersected;

said first insulating film (110) has a plurality of contact holes (110a) disposed in an L-character shape, for respectively connecting end portions of said X-direction conductive wires (112) and of said Y-direction conductive wires (115) of said memory cell array (302) to said functional element section (206) of said second functional block; and

said functional element section (206) of said second functional block is disposed in an L-character shape having two regions extending in directions perpendicular to each other and besides said first functional block (202), but in parallel to two adjacent edges thereof."

Claim 1 of the auxiliary request additionally comprises the features that a random access memory (204) is formed beside the first functional block (202) directly on the semiconductor substrate (100), said random access memory having parallel adjacent edges with respect to the peripheral circuit.

III. The reasoning in the decision of the examining division was essentially as follows:

Main request

The device known from document D5 comprises, above the semiconductor substrate (10), a memory cell array (CM) with a lower layer of conductors (14a) in an X-direction, an intermediate insulation layer (14b) and an upper layer of conductors (14c) in an Y-direction; in the semiconductor substrate, there is a peripheral circuit, comprising an X address decoder (XD), an Y address decoder (YD) and load transistors (20), for reading data from the memory cell array whereby, as shown in Figure 6, the X address decoder (XD) and the Y address decoder (YD) extend in an L-character shape.

The peripheral circuit in the semiconductor substrate (10) is separated from the memory cell array by an insulating film (13) provided with a plurality of contact holes (16) for connecting the peripheral circuit to the memory cell array (CM).

Two features distinguish the semiconductor device of claim 1 from the known device:

(i) the device is specified as comprising a silicon

substrate, and

- (ii) the device is specified as having a peripheral circuit and contact holes disposed in an L-character shape.

Concerning the distinguishing feature (i), it is generally known to be advantageous to use silicon as a substrate for semiconductor devices.

The difference defined in item (ii) in substance amounts to providing an alternative arrangement for the peripheral circuit and the corresponding contact holes already present for reading data while maintaining a small chip area, and this is considered as an obvious alternative.

Therefore, the subject-matter of claim 1 of the main request lacks an inventive step.

Auxiliary request

A further feature distinguishes the semiconductor device of claim 1 of the auxiliary request from that of the device known from document D5 in that:

- (iii) the device is specified as having a random access memory (RAM) formed directly in and on the silicon substrate and having parallel adjacent edges with respect to the peripheral circuit.

However, a rectangular shaped random access memory having parallel edges with respect to memory lines (14a, 14c) is known from document D5 (see Figures 9

and 10 and column 9, lines 42 to 49), ie, with respect to another embodiment in the document. A skilled person wishing to realize a digital computer with a rectangular shaped RAM would form the rectangular shaped RAM in the interior of the substrate in the space which is open for logic and beneath the insulating layer (13).

Therefore, claim 1 of the auxiliary request also lacks an inventive step.

IV. On 11 December 1997, the applicant lodged an appeal against the decision of the examining division, paying the appeal fee on the same day. A statement setting out the grounds of the appeal was filed on 13 February 1998.

V. During the oral proceedings on 5 February 2002, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of

- Main request Claims 1 to 12 according to the main request filed on 7 January 2002 and as amended according to the letter dated 17 January 2002; or
- Auxiliary request claims 1 to 9 filed with the letter dated 17 January 2002.

Claim 1 of the appellant's main request reads as follows:

- "1. A semiconductor device having, on a semiconductor substrate (100), a first functional block (202) for processing data for logical operation and data control, and a second functional block (206, 302)

for previously storing information required for the data processing, wherein

said first functional block (202) has a transistor section (101, 102) formed directly on said semiconductor substrate (100);

said second functional block (206, 302) has a memory cell array (302) located above said transistor section of said first functional block, and a transistor section (104, 105) for forming a peripheral circuit (206) including a decoder, said transistor section of said second functional block also being formed directly on said semiconductor substrate (100);

said transistor section (101, 102) of said first functional block (202) and said transistor section (104, 105) of said second functional block (206, 302) are formed in a lower layer (200) formed on said semiconductor substrate, and said memory cell array (302) is formed in an upper layer (300) provided above said lower layer and separated therefrom by an insulating passivation film (110);

said memory cell array (302) comprising, without including a transistor, a plurality of conductive wires (112) extending in an X-direction, and a plurality of conductive wires (115) extending in an Y-direction, wherein an insulating passivation film (113) is provided between said X-direction conductive wires (112) and said Y-direction conductive wires (115), said X-direction conductive wires and said Y-direction conductive

wires being three-dimensionally intersected when being viewed in a direction substantially perpendicular to an XY plane including said X-direction and said Y-direction, and being electrically interconnected at optional three-dimensional intersections (113a) in accordance with said information previously stored."

Claim 1 of the appellant's **auxiliary request** contains additionally two features at the end of the claim which read as follows:

"wherein

said memory cell array (302) has a substantially rectangular shape; and

said transistor section (104, 105) of said second functional block (206, 302) is formed so as to have a substantially L-character shape having two edges being located slightly outside and below two adjacent edges of said memory cell array (302) so as to face said two edges of said memory cell array."

VI. The appellant submitted in substance the following arguments in support of his requests:

Main request

There is no indication in document D5 that transistors are not to be included in the upper layer (14) above the insulating layer covering the semiconductor substrate and in particular in the memory cell array. Indeed, there are no transistors shown in the upper

layer (14); however, it cannot be concluded from the missing information that there is no transistor in this upper layer. Therefore, since transistors are not excluded in the upper layer of the known device, the subject-matter of the claim is new.

Auxiliary request

The invention as illustrated in principle in Figure 1 of the application provides a specific arrangement of the components of the device: in the upper layer, there is the memory cell array whereas the central processing unit (CPU) and the random access memory (RAM) of the computer together with the L-character shaped peripheral circuit comprising the decoders for the memory cell array, are all in the lower layer. This provides more area for the transistor sections in the lower layer and relatively short interconnections due to the direct connections from the L-character shaped peripheral circuit to the memory cell array, resulting in high speed of information transmission. These last features are not suggested in document D5, so that the subject-matter of claim 1 of the auxiliary request involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request - Novelty*
 - 2.1 A semiconductor device on a semiconductor substrate (10) is known from document D5 (see Figures 1

to 6 and corresponding description) comprising,

a first functional block (the arithmetic section at the bottom of Figure 6) for processing data for logical operation and data control (see column 6, lines 21 to 29),

and a second functional block (14, CM; XD, YD, 20, 21, 22) (see Figure 6; column 6, lines 30 to 40) for previously storing information required for the data processing;

the first functional block has a transistor section (12) formed directly on the semiconductor substrate (10);

the second functional block (14, CM; XD, YD, 20, 21, 22) has a memory cell array (14, CM) located above the transistor section (12) of the first functional block, and a transistor section (XD, YD, 20, 21, 22) for forming a peripheral circuit including a decoder (the X address decoder, the Y address decoder); the transistor section of the second functional block is also formed directly on the semiconductor substrate (see column 4, line 53 to column 5, line 5 and Figure 4);

the transistor section of the first functional block and the transistor section of the second functional block are formed in a lower layer (12) formed on the semiconductor substrate (10), and the memory cell array is formed in an upper layer (14) provided above the lower layer and separated therefrom by an insulating passivation film (13) (see Figure 6 and column 6, lines 21 to 40);

the memory cell array (CM) comprises a plurality of conductive wires (14a) extending in a first direction, a plurality of conductive wires (14c) extending in a direction orthogonal to the first direction, and an insulating passivation film (14b) formed between the conductive wires in the first direction and the conductive wires in the orthogonal direction; the conductive wires in the first direction and the conductive wires in the orthogonal direction are three-dimensionally intersected when being viewed in a direction substantially perpendicular to a plane including these two orthogonal directions, and are electrically interconnected at optional three-dimensional intersections (15) in accordance with the information previously stored.

The appellant argued that **a core feature** of the present invention is that the memory cell array provided in the upper layer does not include a transistor. Neither document D5 nor any of the other prior art documents disclose or suggest such a structure. In particular, the lack of information in document D5 cannot be utilized to conclude that there is no transistor in the upper layer.

However, it is to be noted that there is no transistor disclosed in the functional means in the upper layer of the device known from Figures 1 to 6 of document D5. Also, the transistors which are referred to in this document (see in particular column 4, line 59 to column 5, line 5 and column 6, line 66 to column 7, line 5; Figures 4 to 6) are provided in the lower layer (12) directly on the semiconductor substrate; in particular, the transistors (20) and (21) are mentioned as lying beneath the insulating layer (13) and as being

a portion of the transistors (12) formed directly on the semiconductor substrate. The circuit for the X and Y address decoders including transistors (22), is mentioned as having its outputs coupled to memory (14) through apertures (16).

Therefore, the appellant's arguments are not convincing.

Consequently, the subject-matter of present claim 1 is not distinguished from the device known from Figures 1 to 6 of document D5 and thus lacks novelty in the sense of Article 54 EPC.

Therefore, claim 1 of the main request is not allowable (Article 52(1) EPC).

3. *Auxiliary request*

3.1 Novelty

All the features of claim 1 of the auxiliary request which are recited in claim 1 of the main request, ie are derivable from Figures 1 to 6 and the corresponding text of document D5 (see item V of the Summary of Facts and Submissions and item 2 of the reasons).

Moreover, in the device known from Figure 6 of document D5 (see also Figure 4), the memory cell array (14, CM) is shown as having a substantially rectangular shape. Furthermore, it is shown in Figure 6 of document D5 (see in particular column 6, lines 21 to 40), which is mentioned as illustrating a preferred physical layout for the control section of the computer, that the X address decoder (XD) and the Y address decoder

(YD) of the second functional block (14, CM; XD, YD, 20, 21, 22) are arranged in a substantially L-character shape having two edges located so as to face said two adjacent edges of the memory cell array (14, CM).

However, in the known device (see column 6, line 66 to column 7, line 5), the memory cell array (CM) overlies, in addition to the arithmetic section, ie the transistor section of the first functional block ie the decoders (XD) and (YD). Thus, the transistor section (XD, YD, 20, 21, 22) of the second functional block (14, CM; XD, YD, 20, 21, 22), and in particular the arrangement of the X and Y address decoders (XD) and (YD) with its substantially L-character shape, is not derivable as having two edges located slightly outside and below two adjacent edges of the memory cell array (14, CM) so as to face the two adjacent edges of the memory cell array, as specified in claim 1.

Therefore, since the further prior art documents are less relevant, the subject-matter of claim 1 is not comprised in the state of the art and is thus new in the sense of Article 54 EPC.

3.2 Inventive step

Starting from the device known from Figure 6 of document D5 with the substantially L-character shape formed by the X and Y address decoders (XD) and (YD), to arrive at the device according to claim 1 of the auxiliary request, it is necessary to arrange the transistor section of the second functional block (XD, YD, 20, 21, 22) in accordance with an alternative design, in such a way that this transistor section (XD, YD, 20, 21, 22) of the second functional

block (14, CM; XD, YD, 20, 21, 22) has a substantially L-character shape with two edges being located slightly outside and below two adjacent edges of the memory cell array (14, CM) so as to face the two adjacent edges of the memory cell array.

However, in the Board's judgment, as convincingly set forth in the decision under appeal, for the person skilled in the art, transferring the transistors of the transistor section of the second functional block to arrive at an arrangement wherein the edges of the L-character-shaped transistor section are located outside the edges of the memory cell array is an obvious alternative to the known arrangement.

Therefore, the subject-matter of claim 1 of the auxiliary request is obvious having regard to the state of the art and thus lacks an inventive step in the sense of Article 56 EPC.

4. Consequently, the application is not allowable (Article 97(1) EPC).

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla