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**D E C I S I O N**  
**of 28 August 2002**

**Case Number:** T 0187/98 - 3.4.3

**Application Number:** 91308598.1

**Publication Number:** 0478241

**IPC:** H01L 23/495

**Language of the proceedings:** EN

**Title of invention:**

Insulated lead frame for integrated circuits and method of  
manufacture thereof

**Applicant:**

TEXAS INSTRUMENTS INCORPORATED

**Opponent:**

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**Headword:**

-

**Relevant legal provisions:**

EPC Art. 56, 84

**Keyword:**

"Inventive Step (no - main, first and second auxiliary  
request)"

"Lack of support in the description for a combination of  
different embodiments (third auxiliary request)"

**Decisions cited:**

-

**Catchword:**

-





**Case Number:** T 0187/98 - 3.4.3

**D E C I S I O N**  
**of the Technical Board of Appeal 3.4.3**  
**of 28 August 2002**

**Appellant:** TEXAS INSTRUMENTS INCORPORATED  
13500 North Central Expressway  
Dallas, Texas 75265 (US)

**Representative:** Legg, Cyrus James Grahame  
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20 Red Lion Street  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 8 October 1997  
refusing European patent application  
No. 91 308 598.1 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** V. L. P. Frank  
M. B. Günzel

## Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division dated 8 October 1997 refusing the European patent application No. 91 308 598.1 on the ground that the subject-matters of claims 1 to 3 lacked an inventive step (Article 56 EPC) having regard inter alia to the following prior art documents:

D1: Patent Abstracts of Japan, vol. 12, no. 449  
(E-449) & JP-A-63 177543

D2: Patent Abstracts of Japan, vol. 12, no. 435  
(E-683) & JP-A-63 169747

D6: EP-A-0 354 056

D7: Patent Abstracts of Japan, vol. 13, no. 201  
(E-757) & JP-A-01 023558

II. The appellant (applicant) lodged an appeal on 11 December 1997, paying the appeal fee the same day. The statement setting out the grounds of appeal was filed on 9 February 1998 requesting the grant of a patent on the basis of the claims on file. Oral proceedings were requested in the event that this request could not be granted.

III. In a communication pursuant to Article 11(2) Rules of Procedure of the Boards of Appeal, annexed to the summons for oral proceedings, the Board informed the appellant of its provisional opinion that the subject-matters of claims 1 to 3 did not involve an inventive step.

IV. With the letter dated 26 July 2002 the appellant submitted an amended main request and first to third auxiliary requests, as well as declarations by

Dr. Steven Wright of Imperial College, London and of Ms. Katharine Heinen, one of the inventors of the application in suit, and English translations of documents D1, D2 and D7 (in the following these documents will be referred to as documents D1a, D2a and D7a).

V. At the oral proceedings held on 28 August 2002, the appellant submitted amended first and third auxiliary requests. The appellant thus requested that the decision under appeal be set aside and a patent be granted on the basis of one of the following requests:

*Main Request:* claims 1 to 3 of Annex A filed with the letter of 26 July 2002;

*1st Auxiliary Request:* claim 1 of Annex B' filed during the oral proceedings;

*2nd Auxiliary Request:* claims 1 to 3 of Annex C filed with the letter of 26 July 2002; and

*3rd Auxiliary Request:* claims 1 to 3 of Annex D' filed during the oral proceedings.

VI. The independent claims 1 according to these requests read as follows:

*Main request:*

"1. A method for forming an encapsulated semiconductor device (10), comprising the steps of:

providing a semiconductor die (11) having an active face and a backside;  
positioning a die support pad (12) with a top of said die support pad (12) adjacent to said backside of said semiconductor die (11); and  
depositing a surface of oxide coating (13) to the other side of said die support pad to promote adhesion with a package (10) to encapsulate said semiconductor device;  
characterized by controlling the deposition apparatus to roughen the surface of the said oxide coating (13)."

*1st auxiliary request:*

- "1. A method for forming an encapsulated semiconductor device (10), comprising the steps of:  
providing a semiconductor die (11) having an active face and a backside;  
positioning a die support pad (12) with a top of said die support pad (12) adjacent to said backside of said semiconductor die (11); and  
depositing a surface of oxide coating (13) to the other side of said die support pad to promote adhesion with a package (10) to encapsulate said semiconductor device;  
characterized in that in the deposition plasma provides heat to powder particles and the plasma and powder are propelled towards the die support pad, and by controlling the deposition apparatus to roughen the surface of the said oxide coating (13)."

*2nd auxiliary request:*

"1. A method for forming an encapsulated semiconductor device (10), comprising the steps of:  
providing a semiconductor die (11) having an active face and a backside;  
positioning a die support pad (12) with a top of said die support pad (12) adjacent to said backside of said semiconductor die (11); and  
depositing a surface of oxide coating (13) to the other side of said die support pad to promote adhesion with a package (10) to encapsulate said semiconductor device;  
characterized by controlling the deposition apparatus to roughen the surface of the said oxide coating (13) and to provide a thickness of the oxide coating of between 0.0005 inches (12.5  $\mu\text{m}$ ) and 0.05 inches (1.25 mm)."

*3rd auxiliary request:*

"1. A method for forming an encapsulated semiconductor device (10), comprising the steps of:  
providing a semiconductor die (11) having an active face and a backside;  
positioning a die support pad (12) with a top of said die support pad (12) adjacent to said backside of said semiconductor die (11); and  
depositing a surface of oxide coating (13) to the other side of said die support pad to promote adhesion with a package (10) to encapsulate said semiconductor device;  
characterized by controlling the deposition apparatus to roughen the surface of the said oxide coating (13) and to provide a thickness of the oxide coating of between 0.0005 inches (12.5  $\mu\text{m}$ ) and 0.05 inches (1.25 mm),

and in that the semiconductor device has a lead finger, a power supply bus lying between a terminal of the semiconductor circuit and the lead finger, and a connecting means for connecting the terminal of the semiconductor circuit to the lead finger that crosses the power supply bus, wherein the said deposited oxide coating (13) also insulates the power supply bus from connecting means."

VII. The arguments of the appellant in favour of inventive step can be summarized as follows:

The application addresses the problem of package cracking during the attachment of integrated semiconductor packaged devices to a printed circuit board. The heat generated during reflow soldering converts into steam any moisture present in the package. The elevated steam pressure can cause delamination and cracking of the package. It is thus required to increase the adhesion between the lead frame and the encapsulant. To achieve this increase two different approaches can be recognized in the prior art:

- (i) mechanical or chemical roughening of the lead frame's surface in contact with the encapsulating resin for increasing the surface area available for adhesion to the resin. This is the approach disclosed in documents D6 and D7.
- (ii) provision of a thin oxide interlayer (only some  $\mu\text{m}$  thick) between the lead frame and the encapsulant for increasing the adhesion by chemical interaction (hydrogen bonding). This approach is



disclosed in documents D1 and D2.

A combination of these two different approaches would not be regarded as obvious by a person skilled in the art. Moreover, such a combination would lead to the formation of a thin oxide layer on the mechanically or chemically roughened surface of a lead frame. This is clearly different from the solution proposed in the application in suit which consists in the formation on the lead frame of a thick oxide layer having a rough surface. This approach provides a much larger surface area for attachment and, consequentially, an increased adhesion between the lead frame and the encapsulant than what was obtained in the prior art, since mechanical or chemical roughening of the lead frame produces only a coarse rough surface.

Moreover, the application of the plasma spray deposition process for depositing the oxide layer on a lead frame is an invention in itself, since this technique is not usually employed in the manufacturing of semiconductor integrated circuits and provides a cheap, reliable and fast method for forming the thick oxide layers required for large surface roughness, since obviously a layer's roughness can never be larger than the layer's thickness.

### **Reasons for the Decision**

1. The appeal is admissible.
2. The amendments made to the claims of the main, first and second auxiliary request will not be discussed here in detail, as the subject-matters of these claims is

not allowable for the reasons which follow.

3. *Main request - Inventive step.*

3.1 It is not in dispute that document D2 represents the closest state of the art.

This document addresses the problem of improving adhesion between an integrated circuit's lead frame and the encapsulating resin to avoid the formation of cracks in the encapsulant due to thermal stresses. To this effect, a fine ceramic coating film is deposited on the front and rear surface of the lead frame by plasma spraying, chemical (CVD) or physical vapour deposition (PVD). The ceramic coating film may be made of single or mixed oxides or non-oxide ceramic materials. According to this document, the bonding force between the frame and the resin is increased due to the formation of strong hydrogen bonds between the resin and the ceramic material. No reference, however, is made in this document to the roughness of the coating film (cf. D2a, pages 3 and 4).

3.2 The method according to claim 1 differs therefore from the method disclosed in document D2 in that the deposition apparatus is controlled to roughen the surface of the oxide coating.

According to the application in suit a rough oxide surface promotes adhesion to and reduces the cracking of the encapsulant during the reflow soldering step (cf. page 1, lines 56 to 58 of the published application).

3.3 Document D7 discloses that chemically etching the rear

side of a die pad before encapsulating it with a sealing resin roughens its surface and increases the effective area for adhesion. The cohesion between the sealing resin and the rear surface of the die pad is thereby improved (cf. D7a, page 6, first paragraph).

It is also disclosed in document D6, although without providing any details, that the surface of the die pad was formed to be relatively rough in order to enhance the bonding strength to the encapsulant (cf. D6, column 3, lines 37 to 40).

The skilled person thus learns from these documents that the area of contact between a lead frame and an encapsulant can be increased by roughening the back surface of the lead frame and that the increased contact area improves the adhesion between the lead frame and the encapsulant.

- 3.4 The appellant submitted that a direct combination of the disclosures of documents D2 and D7 would lead to a method in which the lead frame's surface is roughened to increase its area of contact and that afterwards a fine oxide coating is deposited on the roughened surface to further increase the adhesion strength by means of chemical bonds between the coating and the encapsulating resin (cf. document D2a, page 5, penultimate paragraph).
- 3.5 There are, however, two alternative ways for increasing the effective area of the lead frame in contact with the resin. One alternative, as pointed out by the appellant, is to roughen the surface of the lead frame itself, and the other is to interpose an interlayer having a large surface area between the lead frame and

the encapsulant. The second alternative is a viable approach suggested by document D2, since it proposes *inter alia* a plasma spraying method for forming the oxide coating layer. This method involves the softening of particles of a heat fusible material by passing it through a plasma formed by an electric arc and propelling the softened material in particulate form against the surface to be coated. The coating has, by virtue of the deposition of the material in particulate form, a rough surface. The degree of surface roughness can be controlled eg. by varying the size or the feeding rate of the powder particles, or by adjusting the distance between the plasma nozzle and the surface to be coated.

- 3.6 According to the appellant, since document D2 discloses the deposition of a 'fine' oxide coating on the lead frame, a skilled person would only have tried to deposit a thin layer. Although this document does not disclose the coating's thickness, a skilled person would have understood the reference to a 'fine' coating as meaning a thin layer, since document D1, which also addresses the problem of increasing the adhesion between the lead frame and the encapsulant, discloses the deposition of an alumina film having a thickness of at most 1.5  $\mu\text{m}$ . Moreover, the alumina film has to be thin, since it avoids the formation of gold-aluminum intermetallic compounds which could lead to the breaking of the bonding wires (cf. D1a, page 7, last paragraph and page 9, second paragraph).

A thin oxide layer as employed in document D2, however, cannot be rough, since its roughness is limited to the thickness of the coating. Moreover, in the preferred embodiment disclosed in document D2 an alumina coating

is deposited by CVD, a relatively slow deposition method which forms very smooth coatings. In contrast to plasma spraying, a coating formed by CVD is built up by successively depositing molecular layers. Its roughness is, therefore, limited to a molecular scale. For these reasons, the skilled person would not have seriously contemplated to employ a plasma spraying process when following the teaching of document D2.

- 3.7 The Board, however, cannot agree with this argument, since plasma spraying is mentioned in document D2 as a suitable method for forming the oxide coating. The limitation of the disclosure of a prior art document only to its preferred embodiment would, however, contradict the established case law according to which the disclosure of a prior art document comprises any reproducible technical teaching described in it (cf. Case law of the Boards of Appeal of the European Patent Office, 4th ed. 2001, page 60, 2.7).

Although the Board accepts that document D2 when read in combination with document D1 suggests the use of a thin oxide coating, the appellants submission that the use of a thin oxide film rules out its formation by the plasma spraying process cannot be followed. On the contrary, in the Board's view the skilled person deduces from document D2 that the plasma spraying process which necessarily produces a rough surface (as compared to the surface produced by eg CVD) is a suitable process for the deposition of the oxide film.

The Board concurs with the appellant that plasma spraying is not a deposition method commonly employed in the semiconductor manufacturing field. However, in circumstances where the skilled person is prompted by

the problem confronting him to look for solutions in another relevant technical field, the 'skilled person' is a team of experts in different technical fields (cf. Case law of the Boards of Appeal of the European Patent Office, 4th ed. 2001, page 111, 5.1.2). In the present situation an engineer specialized in designing packages for integrated circuits, faced with the disclosure of document D2, would have consulted a specialist in the field of plasma spraying deposition and would have learned that the coatings obtained by this deposition method have inherently a much larger roughness than the layers obtained by CVD or PVD and have, consequently, a much larger effective area onto which the encapsulating resin can adhere. Moreover, he would realize that the surface roughness can be increased with a view to increase the contact area by controlling the process conditions.

For these reasons, it is the judgement of the Board that the subject-matter of claim 1 according to the main request does not involve an inventive step.

4. *First auxiliary request - Inventive step.*

Claim 1 according to this request specifies in addition to the features of claim 1 according to the main request that the oxide coating is deposited by plasma spraying. As already mentioned, however, document D2 discloses plasma spraying as a method suitable for forming the oxide coating.

The subject-matter of claim 1 does therefore not involve an inventive step for the reasons given in respect of claim 1 of the main request.

5. *Second auxiliary request - Inventive step.*

Claim 1 according to this request specifies in addition to the features of claim 1 according to the main request that the thickness of the oxide coating is between 12.5  $\mu\text{m}$  and 1.25 mm.

No special or surprising effect is, however, disclosed in the application in relation with this thickness range. Although coatings employed in the semiconductor manufacturing field are usually only some micrometers thick as in document D1, the requirement of increasing the roughness of the surface's coating makes thicker coatings inevitable.

The Board considers, therefore, that a skilled person would choose the thickness of the oxide coating having regard to the circumstances. In particular, as there are no difficulties in achieving the claimed thickness range by plasma spraying.

For these reasons and the ones discussed in relation to the main request, it is the judgement of the Board that the subject-matter of claim 1 according to this request does not involve an inventive step.

6. *Third auxiliary request*

6.1 Claim 1 according to this request differs from claim 1 according to the second auxiliary request in that it is further specified that the oxide coating also insulates the power supply bus of a Lead-on-Chip (LOC) lead frame from the bonding wires.

6.2 An encapsulated semiconductor device forming the

subject-matter of claim 1, having the rear surface of the die pad covered by an oxide coating for increasing adhesion between the die support pad and the encapsulant, and having an LOC lead frame in which the power supply bus is covered by a dielectric coating is disclosed in claims 4 and 5 as originally filed. Consequently, the requirement of Article 123 (2) EPC is fulfilled.

6.3 A combination of the conventional device as described with reference to Figures 1 and 4 and a LOC device described with reference to Figures 2 and 3 is, however, not described in the application in suit, and this has not been disputed by the applicant.

The question therefore arises whether such a combination of a conventional lead frame device and a LOC lead frame device is adequately supported by the description, as required by Article 84 EPC, second sentence.

6.4 A conventional lead frame comprises a centrally located chip support pad 12 on which the semiconductor chip is mounted, and conductive lead fingers 15 provided along the chip's periphery. Wire bonds connect the chip's bonding pads located along the outer edges of the semiconductor chip 11 to the lead fingers. As the chip's bonding pads and the lead fingers are located along the periphery of the chip, the wire bonds do not cross over a bus bar. (cf. page 4, lines 21 to 25 and Figs. 1 and 4 of the published application).

6.5 A LOC lead frame, on the other hand, comprises two parallel spaced power supply busses 28a and 28b running along the middle of the semiconductor chip and several



conductive lead fingers 27 located at the sides of the power supply busses. The bonding wires providing the connections between the bond pads and the lead fingers have to cross over the power supply bus, since the semiconductor chip has centrally disposed bond pads 23 located between the two power supply busses. As the lead frame rests on the chip's active surface 21 and is fixed to it by double sided adhesive tapes 22a and 22b forming a self-supporting structure, no chip support pad is required in this device (cf. page 4, lines 36 to 51 and Figs. 2a and 2b of the published application).

- 6.6 In the application in suit, the problem of contact between the bonding wires and the power supply bus of a LOC lead frame and the problem of increasing the adhesion between the chip support pad of a conventional lead frame and the encapsulant resin are treated separately from each other.

Moreover, a LOC structure is a self supporting structure, not requiring a die support pad (cf. page 4, line 46 of the published application). In the conventional package, on the other hand, a chip support pad is present and the problem of insulating the power supply busses from the bonding wires does not arise, since the bonding wires do not cross over any power supply busses.

Thus, in the Board's view, the conventional lead frame and the LOC lead frame are two totally different lead frame structures with conflicting requirements giving rise to different technical problems. The description does not contain information which would enable a skilled person to combine these different structures with conflicting requirements in a single lead frame

structure as specified in claim 1.

- 6.7 The appellant has argued that a skilled person would consider the provision of a cooling plate at the rear side of a chip mounted on a LOC lead frame. The problems of adhesion between the encapsulant and the cooling plate and of insulating the power supply busses from the bonding wires would both be present in such a device. The method according to claim 1 of the third auxiliary request addresses therefore both problems simultaneously.

The Board, however, cannot concur with the appellant, since the application does not disclose the use of cooling plates, and the claim specifies the presence of a chip support pad and not of a cooling plate (cf. claim 1, third paragraph). The functions of a chip support pad and of a cooling plate are, however, different. The former serves as a platform on which the semiconductor chip is mounted and the second helps in dissipating the heat produced during the functioning of the chip. The requirements imposed on these two devices are different and they can in no way be seen as being interchangeable.

- 6.8 The appellant also referred to several passages in the description in which LOC and conventional packages are mentioned together as benefiting both from the deposition of the oxide coating (cf. page 1, lines 42 to 43, page 5, lines 52 to 55 and page 6, lines 8 to 12 of the published application).

However, these passages refer to the reduction of the encapsulant's cracking and delamination due to the increased adhesion between the lead frame and the

encapsulant. The Board has no doubts that this effect is also achieved in a LOC lead frame in the regions of the power supply bus which are covered by the oxide coating. This effect is, however, under the correct interpretation of the description, limited to the front side of the LOC lead frame where the power supply busses are insulated from the bonding wires.

6.9 For these reasons, in the judgement of the Board, claim 1 according to the third auxiliary request is not supported by the description as required by Article 84 EPC.

**Order**

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:

R. Schumacher

R. K. Shukla