BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen

D E C I S I O N
of 30 March 2000

Case Number: T 1181/97 - 3.5.2

Application Number: 94830125.4

Publication Number: 0674389

IPC: H03K 17/08

Language of the proceedings: EN

Title of invention:
Overload protection circuit for MOS power drivers

Applicant:
STMicroelectronics S.r.l

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Novelty (yes)"
"Inventive step (yes, after amendment)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1181/97 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 30 March 2000

Appellant: STMicroelectronics S.r.l.
Via C. Olivetti, 2
20041 Agrate Brianza (Milano) (IT)

Representative: Cerbaro, Elena, Dr.
STUDIO TORTA S.r.l.
Via Viotti, 9
10121 Torino (IT)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 25 July 1997 refusing European patent application No. 94 830 125.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: M. R. J. Villemin
C. Rennie-Smith

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 94 830 125.4. The reason given for the refusal was that the subject-matter of claim 1 as originally filed lacked novelty, having regard to the following prior art document:

D1: US-A-4 809 122.

II. In reply to observations of the Board, the appellant filed documents in respect of a main request and an auxiliary request. The amended documents relating to the main request comprise:

- claims 1 to 5, received with the letter dated 17 March 2000,

- amended page 1 of the description, original page 6 of the description with an additional page 6a of text for insertion on page 6 and amended pages 7, 8, 9, 10, 15, 16 of the description, all received with the letter dated 24 February 2000; and

- a sheet of drawings comprising Figures 1 to 4, received with the letter dated 24 February 2000.

Pages 2 to 5, 11 to 14 and 17 of the description as filed remain unamended.

III. Claim 1 of the main request is worded as follows:

" An overload protection circuit (10) for a power MOS

transistor driver (1) having a control terminal (G) at a control potential and supplying a drive current (I_D) to a load, said circuit (10) comprising:

- a slow, low-gain regulating loop (11) comprising a first operating element (15; 34-37) operative above a first predetermined voltage threshold corresponding to a first value of the drive current (I_D), the slow, low-gain regulating loop (11) including a measuring element (4) for measuring variations of the drive current (I_D) and for generating a current limiting signal (I_1) for regulating said control potential without turning off said power MOS transistor driver (1);

- a fast, high-gain regulating loop (12) connected in parallel with said slow, low-gain regulating loop (11) and comprising a second operating element (20; 34, 35, 55-58) operative above a second predetermined voltage threshold higher than said first predetermined voltage threshold and corresponding to a second value of the drive current (I_D) higher than said first value, the fast, high-gain regulating loop (12) detecting rapid variations in said drive current (I_D) and generating a rapid control signal (I_2) for rapidly discharging the capacitive gate region of the power MOS transistor driver (1) and rapidly reducing said control potential without turning off said power MOS transistor driver (1)."

Claims 2 to 5 are dependent on claim 1.

IV. The Appellant argued essentially that claim 1 of the

main request now recited two important features of the invention, namely that the first and second loops were operative above first and second thresholds respectively and that the second loop generated a rapid control signal to discharge the gate region of the power MOS transistor driver. These features were not disclosed in D1.

V. The Appellant requested that the decision under appeal be set aside and a patent granted on the basis of the main request (see section II above).

Should the main request be considered not allowable by the Board, the appellant requested that a patent be granted on the basis of the auxiliary request.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 Admissibility of the amendments

The two-part form for claim 1 has been abandoned. This is appropriate because D1 does not disclose the combination of a low-gain slow regulating loop with a high-gain fast regulating loop. The features recited in claim 1 were all disclosed in combination in the application documents as originally filed. Original claims 2 and 3 have been cancelled and original claims 4 to 7, now claims 2 to 5, have been amended to be consistent with claim 1.

In compliance with Rule 27(1)(b), the text to be inserted on page 6 of the description mentions document D1 with a technical comment on the functioning of the circuit disclosed in this document. The description has also been amended to remove inconsistencies.

In the Board's judgement the present form of the application does not infringe Articles 84 and 123(2) EPC.

2.2 Novelty

The prior art document D1 describes an overload protection circuit which does not comprise all the features recited in claim 1. Thus, the subject-matter of claim 1 is novel within the meaning of Article 54 EPC.

2.3 Inventive step

2.3.1 The problem to be solved by the claimed invention is to provide a protection circuit capable of responding rapidly, even in the event of rapid overloading, without turning off the power stage (see page 6, lines 15 to 18 of the application as filed and column 3, lines 53 to 56 of the published application).

2.3.2 The overload protection circuit disclosed in prior art document D1 is not able to solve the stated problem because switching circuits 36 and 82 (see embodiment according to Figure 1) are only operative for turning OFF or ON the power MOSFET 6.

The way of functioning of this known overload

protection circuit teaches away from the solution according to the claimed overload protection circuit which deliberately avoids any off-on operations of the power MOSFET 1. Even if for the sake of argument the person skilled in the art starting from the overload protection circuit disclosed in D1 and faced with the explicit problem of providing a protection "without turning off the power stage" would have thought of removing the timer 58 and the circuit including transistors 62, 70 from the overload protection circuit disclosed in D1 and arranging the circuit so that the outputs of comparators 44 and 88 would be continuously connected to the gate G of the power MOSFET 6 (see Figure 1), he would have arrived at a protection circuit comprising three loops of a non ON/OFF type. However, these modifications would have led to a circuit still lacking the combination of the essential features recited in claim 1, in particular:

- a slow, low-gain regulating loop comprising a first operating element operative above a first predetermined voltage threshold corresponding to a first value of the drive current,

- a fast, high-gain regulating loop connected in parallel with the slow, low-gain regulating loop and comprising a second operating element operative above a second predetermined voltage threshold higher than the first predetermined threshold and corresponding to a second value of the drive current higher than the first value, the fast, high-gain regulating loop detecting rapid variations in the drive current and generating a rapid control signal for rapidly discharging the

capacitive gate region of the power MOS transistor driver 6 and rapidly reducing the control potential of this driver.

In the Board's judgement these essential features are not obviously derivable from D1. In particular, there is no suggestion in D1 that the circuit described in this document could be further modified in such a manner that the occurrence of a high transient state of the drive current could cause a fast loop to discharge rapidly the capacitive gate region of the power MOS transistor driver 6. Furthermore, if the device 28 of the overload protection circuit known from D1 may be regarded as a fast regulation unit, the delayed-operation protection device 82 can be defined neither as a regulator, since it turns off the controller driver without regulating action, nor as a slow operating device, since no deduction may be made about the speed of this circuit 82 in comparison to the speed of device 28.

2.3.3 In conclusion, the subject-matter of claim 1 of the main request involves an inventive step with regard to the overload protection circuit known from document D1. The documents cited in the European search report are categorised as relating to the technological background (category A).

3. Since the main request is allowable, it is not necessary to examine the auxiliary request.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents mentioned in the appellant's main request:

Claims: No. 1 to 5 filed with the letter dated 17 March 2000.

Description: Pages 2, 3, 4, 5, 11, 12, 13, 14, 17 as originally filed; page 6 with an additional page 6a of text for insertion on page 6, filed with the letter of 24 February 2000, amended pages 1, 7, 8, 9, 10, 15, 16 filed with the letter of 24 February 2000.

Drawings: Figures 1 to 4 filed with the letter of 24 February 2000.

The Registrar: The Chairman:

M. Hörnell W. J. L. Wheeler