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D E C I S I O N
of 3 June 2002

Case Number: T 1169/97 - 3.4.3

Application Number: 92300687.8

Publication Number: 0498550

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:

Method of manufacturing via holes for multilayer
interconnection of semiconductor devices

Applicant:

FUJITSU LIMITED

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step (yes)"

Decisions cited:

-

Catchword:

-



Case Number: T 1169/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 3 June 2002

Appellant: FUJITSU LIMITED
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 24 July 1997
refusing European patent application
No. 92 300 687.8 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
M. J. Vogel

Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division dated 24 July 1997 refusing the European patent application No. 92 300 687.8. The ground for the refusal was that the subject-matter of the claims did not involve an inventive step (Article 56 EPC), having regard to the following prior art documents:

D1: Journal of Vacuum Science & Technology B,
volume 7, No. 1, January/February 1989,
page 127-128, and

D3: EP-A-0 388 563

II. The appellant (applicant) lodged an appeal on 25 September 1997, having paid the appeal fee two days before. The statement setting out the grounds of appeal was filed on 25 November 1997.

III. In response to a communication from the Board, the appellant filed on 8 May 2002 a revised page 4 of the description and revised claims 1 to 5.

The wording of the only independent claim 1 is as follows (emphasis added by the Board for showing the amendments with respect to claim 1 as originally filed)

"1. A method of manufacturing a semiconductor device having conductive layers connected by conductive plugs formed in via-holes, the method including the steps of:

forming via-holes in an interlayer insulating film provided on an underlying conductive layer,

depositing a **continuous** first metal film along the top surface of the interlayer insulating film and the inside of the via-holes by a chemical vapour deposition (CVD) process,

depositing a second metal film on the first metal film by a physical vapour deposition (PVD) process, and

melting the first and second metal films to form conductive plugs in the via-holes **by an appropriate heating means**, to thereby fill the via-holes with the metal material from the outside thereof."

IV. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following patent application documents:

Claims: 1 to 5 filed on 8 May 2002 with the letter dated 7 May 2002
6 to 8 filed on 25 November 1997 with the letter dated 21 November 1997

Description: pages 1, 2 and 6 to 17 as originally filed
pages 3 and 5 filed on 26 May 1995 with the letter dated 23 May 1995
page 4 filed with the letter dated 7 May 2002

Drawings: Sheets 1/8 to 8/8 as originally filed

V. In the decision under appeal the examining division

argued essentially as follows:

Document D3 is the closest state of the art. The subject-matter of claim 1 differs from the method disclosed in this document essentially in that the first and second metal film are melted so that the via-holes are filled with the metal of these films. The technical problem addressed by the invention is, therefore, to completely fill narrow via-holes with metal, while achieving a planarized upper surface. The step of melting both metal layers was, however, known from document D1 and it would have been obvious to a skilled person to use the melting technique known from this document in the method according to document D3 to fill the via-holes with metal (a closely analogous situation).

V. The appellant argued essentially as follows in support of his request:

Document D3 addresses the same problem as the application in suit, ie to connect two conducting layers through a via hole. The method of document D3, however, involves several steps: to taper the sidewalls of the via hole and to deposit a first layer by a CVD process that assures the electrical connection between the two conducting layers. The second metal layer does not have the function of connecting these layers, but only provides the upper conducting plane. Moreover, in this document it is specifically stated that voids which may remain in the via hole are not regarded as being a problem, since the interconnection is assured by the first metal film.

Moreover, there is no reason to combine the teaching of

this document with that of document D1.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

Claim 1 differs from the claim as originally filed in that

(a) the expression "depositing a continuous first metal film" replaces the expression "depositing a first metal film continuously" which was employed originally, and in that

(b) the melting of the first and second metal films is done by "an appropriate heating means" instead of "by an irradiation of an energy means".

The first amendment provides consistency with the description, since the application consistently requires that the first metal film should be continuous (cf. column 4, lines 48 to 57 and column 5, lines 24 to 26, 35 to 36 and 45 to 46 of the published application). However, the expression "continuously" used previously qualified the deposition process, but not the film itself.

The second amendment is disclosed in column 2, lines 55 to 56 and column 5, lines 49 to 51 of the published application.

The description was amended to reflect the amendments

made to the independent claim.

Consequently, the Board is satisfied that the amendments fulfill the requirements of Articles 84 and 123(2) EPC.

3. *Inventive step*

The only remaining issue in this appeal is that of inventive step.

3.1 The application in suit addresses the problem of interconnecting two conductive layers separated by an interlayer insulating film through via-holes. Such structures are commonly used in the manufacturing of semiconductor devices. However, due to the trend to higher integration of these devices the sizes of the via-holes have been reduced and their aspect ratios increased. Metal films formed by physical vapour deposition (PVD) processes produce unsatisfactory step coverage due to the shadow effect and the obtained metal films are discontinuous within the via-hole. On the other hand, chemical vapour deposition (CVD) processes are free of the shadow effect and form continuous metal film within the holes. However, since an organometallic compound gas is generally used in CVD processes, the metal films contain carbon which increases their resistivity.

3.2 It is common ground that document D3 represents the closest state of the art. This document discloses a method of interconnecting two conducting layers through a via-hole. The disclosed method comprises successively the following steps: formation of a tapered oxide layer on the sidewalls of the via hole to improve step

coverage, formation of a titanium barrier layer 30 over all the exposed surfaces, formation by CVD of a thin conformal layer of tungsten disilicide 32, and finally, formation by PVD of an aluminum layer 38 (cf. column 2, lines 3 to 35; column 7, lines 14 to 30 and Figure 7).

According to this document, the electrical interconnection between the upper and lower conducting layers within the via-hole is assured by the conformal titanium nitride and tungsten disilicide layers 30 and 32 (cf. column 6, lines 47 to 52 and column 6, line 56 to column 7, line 4). For this reason, the possibility of voids remaining within the via-hole 14 is not regarded as a problem (cf. column 6, line 30 to 52).

3.3 The method of claim 1 differs from the above prior art method in that the two metal layers are melted, to thereby fill the via-holes with the metal material from the outside of the via-hole.

3.4 According to the application in suit, the effect achieved by this measure is that part of the material of the molten second metal film located on the outside of the via-hole is mass-transported into the via-hole by the presence of a continuous first metal film which acts as a guide for the flow of material (cf. column 4, lines 34 to 44). A further effect achieved by this measure is to planarize the surface of the upper conductive layer in the region overlaying the via-hole (cf. column 6, lines 42 to 44).

For these reasons, the problem addressed by the application in suit having regard to the prior art document D3 is the one originally stated, namely the

provision of a method for fully filling a via-hole with a metal material and to planarize the top surface of it (cf. column 2, lines 43 to 49).

3.5 The examining division, in the decision under appeal, argued that melting a metal layer by laser irradiation to fill a via-hole and to planarize the top surface overlaying the via-hole was known from document D1 (cf. page 127, left-hand column, penultimate paragraph). The skilled person would, therefore, have added a step for melting the metal layers in the method according to document D3 to eliminate the voids which according to the disclosure of this document may remain inside the via-hole and to planarize the top surface.

3.6 The Board, however, cannot concur with this line of argument. In the Board's view, it would not be obvious to combine the methods of documents D3 and D1, since the nature and purpose of the first and second metal films are very different in these two methods.

Document D1 makes reference to a previous work by Mukai et al. in which an aluminum layer was melted by an excimer laser pulse to planarize it. The aluminum layer was covered by a thin copper layer to increase the optical absorption of the laser light (cf. page 127, left-hand column, penultimate paragraph). In the actual experiment reported in this document a thin chromium layer was thermally evaporated on the silicon oxide to promote the adhesion of a thermally evaporated gold layer (cf. page 127, right-hand column, second paragraph 'Experiment'). In both experiments one of the metal layers is not used for electrical conduction, but either to increase absorption of the laser light (the copper layer) or to improve the adherence to the

substrate (the chromium layer). Moreover, this document does not disclose that melting of both the layers is required, since it states that the parameters of the laser pulse were selected to assure that the thermal influence on the layers under the gold layer was kept at a minimum (cf. page 128, right-hand column, end of the second paragraph). As the melting points of gold and chromium are very different (1064 and 1860°C, respectively), it is reasonable to assume that only the overlying gold layer and not the chromium layer was melted by the laser beam.

On the other hand, the first metal film used in document D3 assures the electrical interconnection between the two conducting planes within the via-hole without requiring the continuity of the second metal film in this region. For this reason, the Board concurs with the appellant that it cannot be derived from the combined teaching of documents D1 and D3 that melting the tungsten disilicide and the aluminum layers used in document D3 would improve the electrical properties of the contact. In fact a melting of these two layers could lead to a worsening of the contact, since according to document D3 the electrical contact between the two conducting planes is provided by an intact first metal layer and it cannot be determined beforehand if the resolidification of the molten material would provide such an intact layer.

- 3.7 For the above mentioned reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC and accordingly meets the requirements of Article 52(1) EPC.

The dependent claims concern further particular embodiments of the invention which are patentable for the same reasons.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents:

Claims: 1 to 5 filed on 8 May 2002 with the letter dated 7 May 2002
6 to 8 filed on 25 November 1997 with the letter dated 21 November 1997

Description: pages 1, 2 and 6 to 17 as originally filed
pages 3 and 5 filed on 26 May 1995 with the letter dated 23 May 1995
page 4 filed on 8 May 2002 with the letter dated 7 May 2002

Drawings: Sheets 1/8 to 8/8 as originally filed

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla