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D E C I S I O N
of 26 November 2001

Case Number: T 1141/97 - 3.4.3

Application Number: 90113945.1

Publication Number: 0409256

IPC: H01L 27/10

Language of the proceedings: EN

Title of invention:
Semiconductor IC device and method for manufacturing the same

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2), 56

Keyword:
"Additional subject-matter (no)"
"Inventive step - (yes, after amendments)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1141/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 26 November 2001

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 8 July 1997 refusing European patent application No. 90 113 945.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
J. H. Van Moer

Summary of Facts and Submissions

I. European patent application No. 90 113 945.1 (Publication No. 0 409 256) was refused by a decision of the examining division dated 8 July 1997 on the ground that its subject-matter lacked an inventive step having regard to the documents

D1: GB-A-2 156 581;

D2: EP-A-0 210 397;

D3: Patent Abstracts of Japan, vol. 10, No. 313 (E-448), 24 October 1986; & JP-A-61 125 045, and

D4: US-A-4 737 830.

II. Claim 1 is the only independent claim of the set of 2 claims forming the basis of the decision and it reads as follows:

"1. A semiconductor integrated circuit device comprising:

a semiconductor integrated circuit chip (20) including a semiconductor substrate (31) to which a first power source potential (VDD) is supplied;

at least two cell arrays (5) each extending in a longitudinal direction, and each having a plurality of cells arranged on a major surface of said semiconductor substrate;

a plurality of cell-to-cell wires (8) in a region between said at least two cell arrays, said cell-to-

cell wires extending in the longitudinal direction;

a plurality of dummy wires (4) in the region between said at least two cell arrays, said dummy wires extending in the longitudinal direction and having the same pitch and width as the cell-to-cell wires, and said dummy wires being connected to an internal power source terminal (7) having a second power source potential (VSS) which is different from the first power source potential;

an insulating layer (32) provided between said dummy wires (4) and said substrate (31) such that a capacitance (C) is created by the dummy wires (4), the substrate (31) and their surrounding insulating film (32); and

a connection layer (2) connected to the second power source potential and said dummy wires via a contact hole (3), the connection layer being transverse to the dummy wires;

wherein said dummy wires provide means for stabilizing the second power source potential."

III. The arguments in the decision of the examining division can be summarized as follows:

Both documents D2 and D3 concern devices wherein spare wires or unused wires, which can be termed "dummy wires", remain in integrated circuits after personalizing or correcting the integrated circuit.

The subject-matter of claim 1 differs from any one of the devices according to documents D2 and D3 only in

that:

(a) a first power source potential is applied to the semiconductor substrate, whereas the dummy wires are connected to a second source potential which is different from first potential; and

(b) the connection between the dummy wires and the second power source potential is effected by means of a connection layer and a contact hole, the connection layer being transverse to the dummy wires.

As a consequence of features (a) and (b), the dummy wires and the substrate form together with the intervening insulating layer a capacitance.

The objective problem underlying the claimed subject-matter is to stabilize the second power source potential by reducing voltage fluctuations.

The problem of voltage fluctuations in the power source busses of integrated circuits is known from document D4, which also teaches to connect capacitances to power source busses through a contact hole, the capacitances comprising an electrode on an insulating layer formed on the semiconductor substrate.

Thus, addressing the problem of power source fluctuations in a device known from either document D2 or D3 and applying the solution offered by document D4, it would have been evident for the skilled person to use those spare dummy wires according to documents D2 or D3 which are left unused. This is all the more true as the skilled person would already have had in the

teaching of document D1 an example of dummy wires having the same pitch and width as normal interconnection wires.

Therefore, the subject-matter of claim 1 lacks an inventive step.

IV. The applicant lodged an appeal against this decision on 8 September 1997, paying the appeal fee on the same day. A statement setting out the grounds of the appeal was filed on 7 November 1997.

V. In a communication dated 1 August 2001, the Board of appeal informed the appellant that the appeal did not appear to be allowable, but that a new text of the application, comprising in particular a new amended claim 1 and new amended pages 2 and 9 of the description annexed to the communication, together with the other application documents on file, could meet the objections of the Board.

VI. With a letter dated 10 October 2001, the appellant agreed to the text suggested by the Board.

VII. The appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of the following patent application documents:

Description:
Pages 1, 4 to 8 and 10 as filed
Pages 2 and 9 as annexed to the communication of the Board dated 1 August 2001 and approved by the appellant with the letter dated 10 October 2001;
Page 3 as filed with the letter of 17 March 1997;

Claims:
No. 1 as annexed to the communication of the Board dated 1 August 2001 and approved by the appellant with the letter dated 10 October 2001;
No. 2 filed on 15 April 1997 during the oral proceedings before the examining division;

Drawings:
Sheets 1/4 to 4/4 as filed.

Claim 1 is the only independent claim of the set of 2 claims, and it reads as follows:

"1. A semiconductor integrated circuit device comprising:

a semiconductor integrated circuit chip (20) including a semiconductor substrate (31) to which a first power source potential (VDD) is supplied;

at least two cell arrays (5) each extending in a longitudinal direction, and each having a plurality of cells arranged on a major surface of said semiconductor substrate;

a plurality of cell-to-cell wires (8) in a region between said at least two cell arrays, said cell-to-cell wires extending in the longitudinal direction;

a plurality of dummy wires (4) in **a space portion of** the region between said at least two cell arrays, **which space portion is defined in the region between said at least two cell arrays by the cell-to-cell wires (8),** said dummy wires extending in the longitudinal

direction and having the same pitch and width as the cell-to-cell wires, and dummy wires **of said plurality of dummy wires** being connected to an internal power source terminal (7) having a second power source potential (VSS) which is different from the first power source potential;

an insulating layer (32) provided between said dummy wires (4) and said substrate (31) such that a capacitance (C) is created by the dummy wires (4) **connected to the second power source potential**, the substrate (31) and their surrounding insulating film (32); and

a connection layer (2) connected to the second power source potential and said dummy wires via a contact hole (3), the connection layer being traverse to the dummy wires;

wherein said dummy wires **connected to the second power source potential** provide means for stabilizing the second power source potential**, and the overall shape of the arrangement of the plurality of dummy wires is in accordance with the shape of the space portion defined by the cell-to-cell wires**."

(Emphasis added by the Board to the passages of the claim which are not comprised in claim 1 forming the basis of the decision under appeal).

Moreover, as only further substantial difference with respect to the previous claim, in the paragraph in the middle of the previous claim, in the passage "dummy wires extending in the longitudinal direction and

having the same pitch and width as the cell-to-cell wires, and **said** dummy wires being connected to ...", the word "said" has been deleted, the present passage thus reading "dummy wires extending in the longitudinal direction and having the same pitch and width as the cell-to-cell wires, and dummy wires of said plurality of dummy wires being connected to ...".

VIII. The appellant provided the following arguments in support of his request:

In the present invention, the plurality of dummy wires (4) are formed in a space portion of the region between two cell arrays, the space portion being defined in said region by means of the cell-to-cell wires (8). The overall shape of the arrangement of the dummy wires is in accordance with the space portion defined by the cell-to-cell wires.

Thus, for instance, in Figure 2, the cell-to-cell wires (8) define a space region of a one-step trapezoid shape similar to that of the conventional device shown in Figure 1. To accommodate the overall scheme of the arrangement of the dummy wires to the space portion of the one-step trapezoid shape, the upper dummy wires are short and the middle and lower dummy wires are long, as shown in Figure 2.

Since in this way the space portions are used as dummy wire portions, effective usage of the space portions and reduction in size of semiconductor chip can be achieved. Furthermore, according to the present invention, the dummy wires extend in the same (longitudinal) direction as the cell-to-cell wires, and they have the same pitch and width as the cell-to-cell

wires. Accordingly, the patterning of the dummy cells is easy, resulting in enhancement of the operability of the circuit designing. The above-mentioned features are not disclosed in the cited prior art documents.

Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of the amendments*

2.1 The application concerns a semiconductor integrated circuit device comprising a plurality of cell-to-cell wires and a plurality of dummy wires; the overall shape of the arrangement of the plurality of dummy wires is in accordance with the shape of the space portion defined by the cell-to-cell wires.

Indeed, according to the application as filed (see page 7, lines 16 to 25 and Figure 6), dummy wires are provided at an unoccupied proper area on the connection layout. Moreover, the application as filed (see for instance Figure 2) shows that the arrangement of the plurality of dummy wires (4) is in accordance with the shape of the space portion defined by the cell-to-cell wires (8).

2.2 It is also to be noted that the application concerns a device comprising a plurality of **dummy wires**, and that dummy wires of that plurality of dummy wires are connected to an internal power source terminal (7) having a specific, second power source potential (VSS), which is different from another, already defined first

power source potential which is supplied to the semiconductor substrate of the device; moreover, a connection layer (2) is connected to the second power source potential and said dummy wires.

Indeed, according to the application as filed (see page 5, lines 26 to 35), in the embodiment of the invention illustrated by Figure 2, **all** the dummy wires are connected to the internal power source terminal Vss.

However, according also to the application as filed (see page 6, line 3 to page 7, line 9; see also page 8, lines 21 to 24), there are dummy wires which are mentioned as being used for correction of specific features of the integrated circuit device and which are electrically **cut off** the internal power source terminal Vss; those dummy wires left unused for correction are connected to the internal power source terminal.

Thus, according to the application as filed, there are dummy wires of the plurality of dummy wires connected to the internal power source terminal Vss and dummy wires of the plurality of dummy wires which are needed for correction and which are not connected to the internal power source potential Vss.

2.3 Therefore, the Board is satisfied that the European patent application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed (Art. 123(2) EPC).

3. *Clarity of the claims*

The Board is also satisfied that the claims define unambiguously the matter to be protected and that they are consistent with the description and the drawings, so that they are clear in the sense of Article 84 EPC.

4. The only issue in the present appeal is that of inventive step.

4.1 Document D1 (see Figures 1, 2, 5 and 6 and the corresponding text; see also page 1, lines 75 to 90) concerns a semiconductor memory device with redundant wiring; the device comprises separated cell arrays (2A, ...) and additional wiring, in particular additional word lines (WL_{ADD1}, WL_{ADD2},....) having the same pitch and width as the normal word lines (WL_0, WL_1, ..) interconnecting memory cells formed in rows of the memory device. The additional wiring can be supplied with a fixed potential, e.g. earth potential.

However, it is first to be noted that, in this known device, the word lines (WL_0, WL_1, ..) of the memory cells, i.e. the plurality of cell-to-cell wires, extend over the cell arrays (2A, ...), and thus do not extend in a region between cell arrays (2A, ...) extending in the longitudinal direction, as in the device of claim 1 (cf. in particular page 2, lines 110 to 112).

Moreover, although the additional word lines (WL_{ADD1}, WL_{ADD2},....) are arranged at the ends of the memory cell arrays (2A, ...), they are disclosed as extending within the memory cell arrays (2A, ...), and not between the cell arrays, as in the device of claim 1 (cf. in particular Figure 2).

The additional wiring can be supplied with a fixed

potential, e.g. earth potential or the potential Vcc of 5 volts supplied to one of the electrodes of the capacitor of the memory cells (see page 3, lines 24 to 32; page 3, line 119 to page 4, line 2).

It is also to be noted that, in document D1 (see in particular page 3, lines 24 to 32; page 3, line 119 to page 4, line 2), the fixed potential supplied to the additional word lines (WL_{ADD1}, WL_{ADD2},....), which is e.g. earth potential or the potential Vcc of 5 volts, can be different from the fixed potential supplied to the substrate. It is to be noted in this respect that, since the fixed potential supplied to the additional word lines (WL_{ADD1}, WL_{ADD2},....) is mentioned as being for preventing these additional word lines from floating, no value of the corresponding fixed potential is excluded, so that this fixed potential can be the same as that of the substrate. Thus, contrary to the device of claim 1, electrical conductors can connect the additional word lines (WL_{ADD1}, WL_{ADD2},....) of this known device to the substrate.

4.2 Document D2 (see the whole document, and more in particular Figures 5B and 6 and the corresponding text) concerns a large scale integration (LSI) circuit adaptable for custom design methods; the manufactured circuit, i.e. the adapted integrated circuit, comprises cells and two metal layers (M1) and (M2) for interconnection, whereby the second metal layer (M2) consists of elongated conductors (260, 262, 263,...) which extend in a particular direction; there is a conductive segment (18) for supplying the power connection and a conductive segment (16) for connecting to ground, these conductive segments (16, 18) extending in the direction transverse to that of the second metal

layer (M2).

However, contrary to the device of claim 1, this known device has a first metal layer for interconnection which does not extend in the direction transverse to that of the second metal layer (M2), but which also extends substantially in the same direction as the second metal layer (M2) (see for instance the conductor segments A to E).

Moreover, although some of the wires (for instance D and E) of the first metal layer (M1) are connected to the conductive segment (16) supplying the ground potential, these conductive segments (D, E, ..) are however only derivable as connecting cell components to other cell components or to a terminal (for instance 108), i.e. as forming a specific circuit which also has an earth connection, and not as being for providing means for stabilizing the earth potential, as in the device of claim 1. In this respect, it is to be noted that there is no direct and unambiguous information about the connection of spare parts, in particular remaining spare parts, of the first metal layer (M1).

4.3 A similar device is known from document D3 (see the abstract) which concerns correcting a wrong signal wiring by providing a correcting wiring between signal wirings in an integrated circuit provided with a multilayer interconnection. For reasons similar to those set forth with respect to document D2, document D3 is not relevant to the structure of the appellant's request.

4.4 Document D4 (see column 2, lines 23 to 29; Figure 3A, 3B, 4 to 13 and the corresponding text) concerns an

integrated circuit structure having compensating means for self-inductance effects; the integrated circuit comprises a Vcc bus (4) and a Vss bus (2) having capacitance means (16) coupled between the busses and distributed along the length of the busses. Thus, for instance, the tab (19) of a first electrode (18) of the metal-oxide-semiconductor (MOS) capacitance means (16) is connected to the Vcc bus (4), and the other electrode (24) of the capacitance means (16), i.e. the underlying semiconductor region (24), is connected to the Vss bus (2) by a metal layer (70) overlying the first electrode (18) of the capacitance means and contacting the other electrode (24) through a via in the oxide layer (26). The capacitance means (16) are for reducing the voltage spikes induced during switching. Thus, this known device has compensating means which comprise a first layer for interconnection (18, 19), in particular the first electrode (18) of the capacitance means (16), and a connection layer (70) connected to the Vcc bus (4) (see Figures 5 and 6).

However, contrary to the device of claim 1, this known device has a first layer for interconnection (18, 19) which does not extend in the direction transverse to that of the second metal layer (70, 74, 80), but which also comprises a tab (19) which extends substantially in the same direction as the second metal layer (70, 74, 80) (see in particular Figures 6, 12 and 13).

Moreover, contrary to the device of the claim 1, there is no indication in document D4 that the electrode (18) of the first interconnection layer (18, 19) should extend in the same direction and should have the same pitch and width as the cell-to-cell wirings, and that the overall shape of the arrangement of the plurality

of the electrodes (18) should be in accordance with the shape of the space portion defined by the cell-to-cell wires. In any case, there is no specific information about cell-to-cell wires being in a region between cell arrays of the integrated circuit.

4.5 The further prior art documents are less relevant.

4.6 As mentioned in the appellant's main request (see page 2, penultimate paragraph), an object of the invention is to provide an integrated circuit which can readily prevent an internal power source voltage fluctuation and can additionally readily correct a wrong connection line, or correct an improper signal delay time, with the use of dummy wires .

Moreover, as credibly argued by the appellant, in the claimed device, the space portions defined by the cell-to-cell wires are used for dummy wire portions, and this results in effective usage of the space portions; thus, reduction in size of the semiconductor chip can be achieved. Furthermore, the dummy wires extend in the same (longitudinal) direction as the cell-to-cell wires, and they have the same pitch and width as the cell-to-cell wires. Accordingly, the patterning of the dummy cells is easy, resulting in enhancement of the operability of the circuit designing. The above-mentioned features are not disclosed in the cited prior art documents.

Indeed, starting from document D4, which in the opinion of the Board is the closest prior art document in that sense that it is the only document concerning the prevention of voltage spikes in fixed potential sources of an integrated circuit, there is no incitation in

this document or in the other cited documents to achieve an effective usage of the space portions for stabilization purposes and additionally for other uses of "dummy wires", e.g. for correcting a wrong connection line, as in the claimed device.

The problem addressed in document D2 is personalization of custom circuits, i.e. manufacturing the integrated circuit by personalizing already made standard cells of the integrated circuit, this being done by personalizing two metal layers, inter alia by selective cutting and/or welding. There is no indication about any "dummy wires", or about any particular arrangement of the cell arrays or of the cell-to-cell wires. Indeed, there are generally known connections of integrated circuit components to fixed potential, e.g. ground. However, there is no indication of any stabilizing means connected to said fixed potentials.

Similar considerations apply to document D3, which concerns correcting a wrong signal wiring.

Document D1 is less relevant in the sense that the additional word lines (WL_{ADD1}, WL_{ADD2},....) are for a different purpose, i.e. avoiding problems associated with the processing of resist during device fabrication. The fixed potential supplied to the additional word lines (WL_{ADD1}, WL_{ADD2},....) is mentioned as being for preventing these additional word lines from floating, whereby any fixed potential may be used. Avoiding fluctuation of a fixed potential is not derivable. Moreover, the arrangement of the cell-to-cell wires and additional and redundant circuit wirings does not correspond to that of the device of claim 1.

4.7 Therefore, in the Board's judgement, having regard to the state of the art, the subject-matter of claim 1 is not obvious to a skilled person, so that it involves an inventive step in the sense of Article 56 EPC.

Consequently, a patent can be granted on this basis (Article 97(2) EPC).

5. Therefore, oral proceedings, which had been requested auxiliarily, are not necessary.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following patent application documents:

Description:
Pages 1, 4 to 8 and 10 as filed
Pages 2 and 9 as annexed to the communication of the Board dated 1 August 2001;
Page 3 as filed with the letter of 17 March 1997;

Claims:
No. 1 as annexed to the communication of the Board dated 1 August 2001;
No. 2 filed on 15 April 1997 during the oral proceedings before the examining division;

Drawings:

Sheets 1/4 to 4/4 as filed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla