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D E C I S I O N
of 20 December 2001

Case Number: T 1088/97 - 3.4.3

Application Number: 92300985.6

Publication Number: 0502614

IPC: H01L 23/522

Language of the proceedings: EN

Title of invention:
Thin film circuit substrate and processes for its manufacture

Applicant:
FUJITSU LIMITED

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56, 123(2)

Keyword:
"Inventive step (yes) after amendment"

Decisions cited:
-

Catchword:
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Case Number: T 1088/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 20 December 2001

Appellant: FUJITSU LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 1 July 1997 refusing European patent application No. 92 300 985.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. B. Guenzel

Summary of Facts and Submissions

I. European patent application no. 92 300 985.6 was refused in a decision of the examining division dated 1 July 1997. The ground for the refusal was that the subject matter of claim 1 filed with the letter dated 28 August 1996 was not new having regard to the prior art documents

D1: US-A-4 931 354; and

D2: IBM Journal of Research and Development, vol. 29, no. 3, May 1985, pages 277 to 288.

In addition, according to the decision, the subject matter of claims 2 to 8 did not involve an inventive step having regard to documents D1, D2, and

D3: 8th IEMT 1990, International Electronic Manufacturing Technology Symposium, 7 to 9 May 1990, Baveno (IT), pages 503 to 507; and

D4: EP-A-0 233 085.

II. The appellant (applicant) lodged an appeal on 29 August 1997, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 20 October 1997 together with new claims.

III. In response to communications of the Board, the appellant filed amended application documents with the letters dated 24 October 2001 and 21 November 2001. The appellant requests that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 7 filed with the letter dated 21 November 2001;

Description: pages 2, 3, and 3a filed with the letter dated 21 November 2001,
pages 1 and 4 to 9 as originally filed;

Drawings: Sheets 1/8 to 8/8 as originally filed.

VI. The claims 1 and 4 to 7 according to the appellant's request read as follows:

"1. A multilayer thin film circuit substrate comprising a plurality of conductor layers (4, 10) separated by an insulator (2, 3), and a conductor (1) for the transmission of signals, the conductor (1) being embedded in a first insulator (2) with the first insulator covering the top and side surfaces of the conductor (1) and at least partly covering the base of the conductor (1), the first insulator (2) being solid and having a low dielectric constant compared to that of a second insulator, the conductor (1) and the first insulator (2) being surrounded entirely by the second insulator (3), the second insulator (3) having a good adhesiveness to the conductor layers (4, 10) compared to that of the first insulator (2)."

"4. A multilayer thin film circuit substrate according to any one of the preceding claims, in which the conductor (1) is supported on only a part of its base by the second insulator (3) and all other parts of its surface is in contact with the first insulator (2)."

"5. A multilayer thin film circuit substrate according to any of claims 1 to 3, in which the conductor (1) is entirely surrounded by the first insulator."

"6. A method of manufacturing a multilayer thin film circuit substrate according to claim 4, comprising the steps of:

forming a conductor (1) on the surface of an insulator layer (3) made of the material of the second insulator;

eliminating, by isotropic etching, the surface of the insulator layer (3) except for a portion thereof supporting part of the base of the conductor (1);

coating the entire surface of the etched insulator layer (3) with another insulator layer made of the material of the first insulator (2);

eliminating, by etching, the other insulator layer (2) remote from the conductor (1); and,

forming a further insulator layer made of the material of the second insulator on the exposed insulator layer (3) and remaining other insulator layer (2)."

"7. A process of manufacturing a multilayer thin film circuit substrate according to claim 5, comprising the steps of:

forming a first insulator layer made of the

material of the first insulator (2) on the surface of a second insulator layer made of the material of the second insulator (3);

forming a conductor (1) on the surface of the first insulator layer (2);

coating at least the surface of the first insulator layer (2) and the conductor with a third insulator layer (2') made of the material of the first insulator (2);

selectively eliminating, by etching, the first and third insulator layers (2, 2') remote from the conductor (1); and,

depositing a fourth insulator (3) layer made of the material of the second insulator on the exposed second insulator layer and remaining first and third insulator layers."

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and Clarity*

Claim 1 contains the features of claim 1 as filed with the addition that (i) the first insulator covers the top and side surfaces of the conductor and at least partly covering the base of the conductor; and that (ii) the first insulator is solid. Feature (i) is based on the embodiments of Figures 1 to 25 clarifying the term "substantially encircled" used in claim 1 as

filed. Feature (ii) is clearly derivable from the description of all the embodiments of the invention in the application as filed, according to which a layer of the first insulator (2) is patterned and etched, ie a process which is only possible when the first insulator is made of a solid material (cf. Figures 6, 14 and 19).

Dependent claims 3 to 5 are based on claims 4, 2, and 3 as filed, respectively. Claims 6 and 7 are based on claims 5 and 7 as filed, respectively.

The claims are furthermore considered clear and concise.

Therefore, the requirements of Articles 123(2) and 84 EPC are met.

3. *Novelty*

3.1 The application in suit relates to multilayer thin film circuit substrates for devices requiring a high signal propagation velocity. It is known that the signal propagation velocity of the conductive paths in a thin film circuit substrate is limited by the capacitive coupling between the paths, and thereby by the dielectric constant å of the (insulating) substrate material. Therefore, different materials having a dielectric constant of about 2.0 have been used instead of the conventional polyimides which have a dielectric constant of about 3.3. Since these materials having a low dielectric constant suffer from problems such as poor adhesion, it has been suggested to use a sandwich substrate where the conductive path is formed between a conventional polyimide and a layer having a low dielectric constant. The reduction in dielectric

constant is however limited, and the problems of adhesion remain.

To solve these problems, the present invention suggests a device where an embedded conductor is covered by a first insulator on its top and side surfaces and at least partly on is base. The first insulator, which has a low dielectric constant, is in turn entirely surrounded by a second insulator having a good adhesiveness to the conductor layers.

3.2 Document D1 discloses a multilayer thin film circuit substrate comprising conductors 3 inside a ceramic substrate 2 (cf. Figure 1). In order to lower the effective dielectric constant and thereby to minimize the propagation loss and delay of signals, the substrate is made of a ceramic having relatively low dielectric constant, and each conductor 3 is formed in a cavity 5 or in a porous medium within the ceramic substrate 2 (cf. column 3, lines 43 to 59, column 4, lines 15 to 27; Figure 1). Each cavity or porous medium covers the respective conductor on its top and side surfaces. The cavities are produced by coating the conductors with a combustive paste which burns and leaves small gaps of cavities during the process of sintering the ceramic substrate in an oven (cf. column 4, lines 35 to 54). The cavities may be filled with a porous ceramic material by mixing ceramic powder and combustible material instead of using a combustive paste.

3.2.1 The device of claim 1 differs from that of document D1 in that the first insulator is a solid and covers not only the top and side surfaces of the conductor, but also covers at least partly the base of the conductor.

In the device of document D1, only the top and side surfaces of the conductor is in contact with the insulator having a low dielectric constant which is either air or a porous ceramic.

3.3 In document D2, the capacitance of wiring structures for VLSI, ie for integrated circuit chips, was investigated. Three different wiring structures were analyzed where the conductors are embedded in different insulators (cf. Figures 6 to 8).

3.3.1 The device depicted in Figure 6 of document D2 comprises conductors covered on all sides by silicon oxide layers which, in turn, are covered on the top by a silicon nitride layer and a polyimide layer. Thus, in contrast to the device of claim 1, the silicon oxide layers are not completely surrounded by a second dielectric having a higher dielectric constant than silicon oxide.

3.3.2 The device shown in Figure 7 of document D2 comprises conductors formed on a silicon oxide layer and covered on the top and side surfaces by a silicon nitride layer, which in turn is covered on the top by a polyimide layer. Thus, in contrast to the device of claim 1, the device of Figure 7 does not have a first insulator which covers the top and side surfaces *and* at least partly the base surface of the conductors.

3.3.3 In the device shown in Figure 8 of document D2, the conductors are embedded in a first insulator made of polyimide. The polyimide layer is formed on a silicon oxide/nitride stacked layer. Thus, the device of Figure 8 does not have a second insulator which entirely surrounds the polyimide, in contrast to the

claimed device.

3.4 Document D3 discloses the properties of Teflon AF having a dielectric constant of 1.89 and suggests that this material should be useful in the electronics industry (cf. page 504).

3.5 Document D4 discloses a ceramic thin film circuit substrate where cavities are running parallel to conductors within the substrate in order to lower the capacitance (cf. abstract; Figure 2). The conductors themselves, however, are completely in contact with the ceramic material.

3.6 Thus, the subject matter of claim 1 is new within the meaning of Article 54 EPC.

4. *Inventive step*

4.1 Document D1 is considered the closest prior art, since it concerns the same type of device, a multilayer thin film circuit substrate, and addresses the same technical problem as the application in suit, ie lowering the parasitic capacitance between the conductors.

4.2 In view of the differences between the device according to claim 1 and that of document D1, the technical problem thus relates to further reducing the effective dielectric constant of the insulator in which the conductors are embedded, without compromising in the adhesiveness of the insulator to the outer conductive layers. This problem corresponds to that addressed in the application as filed (cf. page 3, lines 13 to 16).

4.3 In the decision under appeal, the examining division considered a modification of the device of document D1, wherein the first insulator also covers at least partly the base of the conductor, as falling within the scope of normal design options readily available for the skilled person.

The appellant argued however convincingly that the cavities/porous media around the conductors in the device of document D1 are formed using a combustible paste applied on the conductor layer which burns during a heating step (firing), and it would therefore not be possible to surround the conductor on all sides with the first insulator, since the conductor would not be supported within the substrate. Even when a porous ceramic is used inside the cavities, the porous ceramic would not be able to provide the sufficient mechanical support for the conductor within the substrate: In order to have the desired low dielectric constant, the porous ceramic must have a high proportion of pores, and is therefore not mechanically stable.

4.4 Although other materials for the substrate than ceramics, such as glass epoxy resins and polyimide resins having a relatively high dielectric constant, are mentioned in document D1 (cf. column 2, lines 29 to 39), ceramic is the preferred material and only ceramic substrates are disclosed in the embodiments described in document D1. As a first insulator having a low dielectric constant, only a cavity or a porous medium is disclosed in document D1. Moreover, due to the high temperature 850 to 1000°C involved at the sintering step required to process the ceramic (cf. column 4, lines 48 to 54), it is not apparent whether any solid insulating materials with a low

dielectric constant would be a suitable alternative to the cavity or porous medium used in the device of document D1.

Therefore, in the multilayer circuit substrate disclosed in document D1, the necessary modifications in order to arrive at the claimed device would not be obvious to the person skilled in the art.

4.5 Also the other available prior art documents do not provide any teaching, which in combination with that of document D1, would result in the claimed device.

Therefore, in the Board's judgement, the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents as specified under item III above.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla