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D E C I S I O N
of 7 November 2001

Case Number: T 0916/97 - 3.4.3

Application Number: 91111028.6

Publication Number: 0466014

IPC: H01L 21/322

Language of the proceedings: EN

Title of invention:

External gettering during manufacture of semiconductor devices

Applicant:

KABUSHIKI KAISHA TOSHIBA

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 123(2), 56

Keyword:

"Admissibility of amendments (yes)"

"Inventive step (yes - after amendments)"

Decisions cited:

-

Catchword:

-



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Boards of Appeal

Chambres de recours

Case Number: T 0916/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 7 November 2001

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 26 March 1997
refusing European patent application
No. 91 111 028.6 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
J. H. Van Moer

Summary of Facts and Submissions

I. European patent application No. 91 111 028.6 (Publication No. 0 466 014) was refused by a decision of the examining division dated 26 March 1997 on the ground that the application as amended contained subject-matter extending beyond the content of the application as filed (Article 123(2) EPC).

II. Claim 1 of the main request forming the basis for the decision of the examining division reads as follows:

"1. A method of manufacturing a semiconductor device, comprising

a step of forming a gettering site (3) on a backside of a semiconductor wafer (1):

a step of subjecting said semiconductor wafer to a heat treatment to trap contaminant impurities in the gettering site (3);

a step of removing a contaminated layer of the gettering site in which the contaminant impurities are trapped; and

a step of performing a film formation, a heat treatment, a lithography, or an ion-implantation to form a PN junction of the semiconductor device,

all of said steps constituting one cycle, and said one cycle being repeated."

(Emphasis added by the Board to indicate amendments in

claim 1 in relation to claim 1 of the application as filed).

- III. In the decision, the examining division found that, in the application as filed, there was a basis for a step of performing an ion implantation to form a PN junction of the semiconductor device, but that there was no disclosure of any step of performing a film formation, a heat treatment or a lithography specifically to form a PN junction of the semiconductor device. Moreover, according to the decision, ion implantation is disclosed originally, but not together with all the other features of the claim. Therefore, claim 1 contained additional subject-matter, contrary to the requirement of Article 123(2) EPC.

Moreover, the decision of the examining division contained objections of lack of inventive step having regard to documents

D1: Database WPI, week 7720, AN 77-35380Y &
JP-A-52 044 163,

D2: US-A-4 144 099 and

D3: DD-A-258 681.

- IV. The applicant lodged an appeal against the decision of the examining division on 28 May 1997, paying the appeal fee on 26 May 1997. A statement setting out the grounds of the appeal was filed on 28 July 1997.
- V. During the oral proceedings held on 7 November 2001 the appellant (applicant) filed a new set of 15 claims and requested that the decision under appeal be set aside

and that a patent be granted on the basis of these new claims.

Claim 1 of the appellant's request is the only independent claim and reads as follows:

"1. A method of manufacturing a semiconductor device, comprising:

a step of forming a gettering site (3) **only** on a backside of a semiconductor wafer (1);

a step of subjecting said semiconductor wafer to a heat treatment to trap contaminant impurities in the gettering site (3); and

a step of removing **the gettering site together with** a contaminated layer of the gettering site in which the contaminant impurities are trapped;

all of said steps constituting one cycle, and said one cycle being repeated at least twice;

wherein in any repeated cycle or cycles, respectively, the gettering sites are formed on the entire backside of the wafer; and

wherein between the process of removing the contaminated layer obtained by trapping impurities in the gettering site on the backside of the wafer in a preceding cycle and the process of forming a new gettering site on the backside of the wafer in the next following cycle a step of a normal semiconductor manufacturing process is inserted, said normal

semiconductor manufacturing process comprising a step of performing a heat treatment to form a region or layer (5; 8; 11) of the semiconductor device."

(Emphasis added by the Board to those amendments which distinguish in substance this claim from claim 1 of the application as filed).

VI. The appellant submitted the following arguments in support of his request:

Claim 1 is based on a version which had been considered by the examining division as containing no additional subject-matter. Claim 1 further specifies that, as derivable from the whole content of the application as filed, in each cycle of the method, it is only on the backside of the semiconductor wafer (1) that the gettering site (3) is formed and that, in any repeated cycle or cycles, respectively, the gettering sites are formed on the entire backside of the wafer. Therefore, claim 1 does not infringe against Article 123(2) EPC.

Diffusion of trapped impurities during a processing step is a serious problem in view of device miniaturization. In the method of claim 1, in order to remove the contaminant impurities from the surface of the wafer in which the elements of the miniaturized integrated circuit are to be manufactured, the gettering process is done on the opposite side, ie, the backside of the wafer. Moreover, the gettering process is repeated so as to avoid high temperature and long duration of the gettering process, a long gettering process resulting in the contaminant impurities reaching the front side of the wafer. It is also to be noted that inserting heating steps of normal

semiconductor devices manufacturing processes between gettering cycles increases the yield of the gettering process.

This is not suggested in the prior art:

Document D1 is not relevant since the front surface and the back surface of the wafer are submitted to gettering and removal of gettering sites. Moreover, document D1 does not disclose any heating step of normal semiconductor devices manufacturing process inserted between successive gettering cycles.

The refresh gettering process of document D3 is not relevant since it concerns a process wherein gettering sites are not formed on the entire back side of the wafer and, moreover, wherein there is no step of removing a gettering site together with the contaminated layer.

In document D2, only a layer of the gettering site with the contaminated layer is removed and successive cycles of the gettering operation are not disclosed.

Therefore, the subject-matter of claim 1 is not suggested by the state of the art and thus involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.
2. *Admissibility of the amendments*

Claim 1 is based on claim 1 of the application as filed and the following additional features:

The new feature that, in each cycle of the method, it is only on the backside of the semiconductor wafer (1) that the gettering site (3) is formed is derivable from the whole content of the application as filed, and is shown in particular in Figures 1A to 1I illustrating the only complete embodiment disclosed therein. The same is true of the amendments which require that, in any repeated cycle or cycles, respectively, the gettering sites are formed on the entire backside of the wafer, and that, in each cycle of the method, the gettering site is removed together with a contaminated layer of the gettering site in which the contaminant impurities are trapped (see for instance dependent claim 12; page 4, lines 28 to 34; page 8, lines 3 to 4).

The following is to be noted concerning the last feature of claim 1:

In the application as filed (see page 11, lines 25 to 30), it is stated that, in the above embodiment, a normal semiconductor device manufacture process is inserted between the process of removing the contaminated layer obtained by trapping impurities in the damaged layer, ie in the gettering site on the backside of the wafer and that of forming a new damaged layer on the backside of the wafer. Indeed, in the embodiment illustrated by Figures 1A to 1I, between the process of removing the contaminated layer obtained by trapping impurities in the gettering site (3; 31) on the backside of the wafer in a preceding cycle and the process of forming a new gettering site (31; 32) on the

backside of the wafer in the next following cycle a step of a normal semiconductor manufacturing process is inserted, said normal semiconductor manufacturing process comprising a step of performing a heat treatment to form a region, ie doped source and drain regions (10; 13), or a layer, ie for instance the layers (6, 7) for forming the field oxide film (8) by local oxidation or the interlayer insulation film (11), of the semiconductor device.

It is derivable from the whole content of the application as filed that this particular teaching is not restricted to the particular embodiment illustrated by Figures 1A to 1I.

The Board is satisfied that the amendments to claim 1 therefore comply with the requirement of Article 123(2) EPC.

3. *Clarity*

It is to be noted that the description is still to be adapted to the new claims.

In the opinion of the Board, claim 1 clearly defines the subject-matter to be protected.

Also, it is to be noted that, according to dependent claim 14, a new gettering site is formed at the same time when the gettering site together with the contaminated layer is removed by mechanical grinding. This feature, which was contained in a somewhat different wording in the other independent claim of the main request before the examining division, had been objected in the decision under appeal as not being

supported by the description.

The Board is however of the opinion that, since the description of the application as filed (see page 4, lines 21 to 23) states that "The contaminated layer is removed by mechanical grinding and, at the same time, a new gettering site is formed by the mechanical grinding.", there is sufficient support for said feature and it is not necessary to enter into considerations about the way said technical operation is carried out.

Therefore, the Board is satisfied that the claims are clear in the sense of Article 84 EPC.

4. *Novelty*

4.1 A method of manufacturing a semiconductor device is known from document D1 (see the abstract and the drawings of the corresponding Japanese patent application), comprising:

a step of forming a gettering site (13a, 13b) on a semiconductor wafer (10), this being done by phosphorus diffusion;

a step of subjecting said semiconductor wafer to a heat treatment to trap contaminant impurities in the gettering site, this being done by the heat treatment accompanying the diffusion process; and

a step of removing the gettering site together with a contaminated layer of the gettering site in which the contaminant impurities are trapped;

all of said steps constituting one cycle, and said one cycle being repeated several times, until the lifetime is increased to the desired value;

wherein in any repeated cycle or cycles, respectively, the gettering sites are formed *inter alia* on the entire backsides of the wafer.

However, contrary to the method of claim 1, in the known method,

- (i) the gettering site is not formed only on the backside of the semiconductor wafer, but on both main surfaces of the wafer;
- (ii) no step of a normal semiconductor manufacturing process is inserted, said normal semiconductor manufacturing process comprising a step of performing a heat treatment to form a region or layer of the semiconductor device, is effected between the process of removing the contaminated layer obtained by trapping impurities in the gettering site *inter alia* on the backside of the wafer in a preceding cycle and the process of forming a new gettering site *inter alia* on the backside of the wafer in the next following cycle.

4.2 A method of manufacturing a semiconductor device is also known from document D3 (see the whole document and, in particular, the example), comprising:

a step of forming a gettering site only on a backside of a semiconductor wafer;

a step of subjecting said semiconductor wafer to a heat

treatment to trap contaminant impurities in the gettering site; and

all of said steps constituting one cycle, and said one cycle being repeated several times.

However, contrary to the method of claim 1, none of the cycles of the known method comprises a step of removing the gettering site together with a contaminated layer of the gettering site in which the contaminant impurities are trapped.

In this respect, it is to be noted that, indeed, only the removal of covering layers ("Deckschichten"), such as oxide or nitride layers, is derivable from document D3.

Moreover, contrary to the method of claim 1, the gettering sites formed in the repeated cycle or cycles are not formed on the entire backside of the wafer.

Indeed, it is derivable from the technical teaching of the document that the disclosed gettering effect relies on stress caused by the rands of layers such as silicon nitride layers covering strip-shaped regions of the back side of the wafer, the "gettering refreshment" being necessary and being obtained by repetition of the gettering cycle, whereby initially coated regions are not submitted to such "refreshment".

It is also to be noted that, contrary to the method of claim 1, no step of a normal semiconductor manufacturing process comprising a step of performing a heat treatment to form a region or layer (5; 8; 11) of the semiconductor device, is inserted between the

process of removing the contaminated layer obtained by trapping impurities in the gettering site on the backside of the wafer in a preceding cycle and the process of forming a new gettering site on the backside of the wafer in the next following cycle.

It is to be noted in this respect that, although it is specified in the document (see page 1, the paragraph "Anwendungsgebiet der Erfindung"; see also claim 6) that the method disclosed therein is effected during the process of manufacturing the semiconductor device, the only indication about such process of manufacturing is that it is done during the step of heating during gettering cycles of the method.

4.3 A method of manufacturing a semiconductor device is known from document D2 (see in particular column 1, lines 39 to 63), comprising:

a step of forming a gettering site only on a backside of a semiconductor wafer (1);

a step of subjecting the semiconductor wafer to a heat treatment to trap contaminant impurities in the gettering site; and

a step of removing a contaminated layer of the gettering site in which the contaminant impurities are trapped,

wherein the gettering sites is formed on the entire backside of the wafer.

However, contrary to the method of claim 1, the gettering site of the known process for preparing a

gettered wafer, which is done by damaging the back side, is not removed. Indeed, it is stated that a layer of crystallographic damage adjacent to the face is retained. Moreover, there is no repetition of the steps of the gettering method. Accordingly, there is no step of a normal semiconductor manufacturing process comprising a step of performing a heat treatment to form a region or layer of the semiconductor device inserted between successive cycles of preparing a gettered wafer.

4.4 Therefore, since moreover the further prior art documents are less relevant, the subject-matter of claim 1 does not form part of the state of the art and is thus new in the sense of Article 54 EPC.

5. *Inventive step*

5.1 An object of the present invention is to provide a method of manufacturing a semiconductor device using a new gettering technique which does not suffer from the drawback of the conventional gettering technique wherein the contaminants trapped in the gettering site are released therefrom by the subsequent heat treatment so that the gettering effect is reduced to half or lost by heat treatment (see, in the application as filed, page 3, lines 17 to 21; page 4, line 28 to page 5, line 7; see also page 12, lines 22 to 29). As stated in these passages and as also convincingly argued by the appellant, contaminant impurities can be effectively removed without requiring a high temperature or a long gettering time, this being particularly convenient in the case of a high degree of integration of semiconductor devices whereby miniaturization of semiconductor elements is required. As further credibly

argued by the appellant, for highly miniaturized integrated circuit, in order to avoid remaining damage resulting from the gettering steps, it is important to avoid forming gettering sites in the surface of the wafer on which the semiconductor elements of the integrated circuit are to be formed.

Moreover, as stated in the application as filed (see page 4, line 28 to page 5, line 7; page 9, lines 11 to 21; page 10, lines 25 to 30; page 14, lines 20 to 27; see also page 7, lines 24 to 36 and Figures 1B to 1D), the gettering operations, in particular those comprising a high temperature heating step, can be used before and during the process of manufacturing elements; it is also mentioned that the gettering operation can be efficiently performed using a heat treatment in the process of treating the wafer rather than using a heat treatment exclusively for the gettering operation and that, since the heat treatment used in a manufacturing process can be applied to the gettering operation, yield and reliability of semiconductor devices can be increased.

Therefore, it is derivable from the application as filed that an object of the present invention consists in providing an efficient method of manufacturing a miniaturized semiconductor device using a gettering technique.

- 5.2 In the opinion of the Board, document D3 (see also in particular page 2, the seven last lines) represents the closest prior art document since it also concerns a gettering technique applied only on the back surface of a wafer, ie on the surface opposite to that wherein the microelectronic elements are to be formed.

As discussed in point 4.2 above, in the method according to document D3, after the impurities are trapped at the gettering site, the latter is not removed along with the trapped impurities. Also, in a subsequent gettering step, the **entire** back surface of the wafer is not provided with the gettering site, but regions different from the previous regions are provided with the gettering sites. Thus, there is no repetition of the gettering step as in the present invention.

As also set forth here above, document D1 does not concern a method wherein gettering is effected only on the back side of the wafer. Moreover, there is no indication in the abstract of document D1 about any normal manufacturing step comprising a heat treatment between cycles of gettering of the wafer. Therefore, starting from document D3, document D1 does not provide to the person skilled in the art a teaching convenient for increasing the efficiency of the gettering process, in particular for miniaturized semiconductor devices.

Document D2 is insofar not relevant for solving the object of the invention as it proposes to retain a part of the obtained gettering site layer, this being thus an impediment against any repetition of gettering cycles and, accordingly, against inserting other high temperature treatments comprised in normal semiconductor manufacturing process steps.

5.3 Therefore, starting from document D3, documents D1 or D2 does not lead to the method of claim 1 in an obvious manner, so that having regard to the state of the art, the subject-matter of claim 1 is not obvious to a person skilled in the art and thus involves an

inventive step in the sense of Article 56 EPC.

6. Consequently, a patent can be granted on this basis (Articles 52(1) and 97(2) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent with the following documents:
 - claims 1 to 15 submitted at the oral proceedings;
 - description to be adapted to the claims;
 - Figures as originally filed.

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla