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D E C I S I O N
of 27 April 2001

Case Number: T 0811/97 -. 3.4.3

Application Number: 91306176.8

Publication Number: 0469728

IPC: H01L 27/10

Language of the proceedings: EN

Title of invention:
Programmable interconnect architecture

Applicant:
ACTEL CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Specific combination of features - not rendered obvious by the prior art"

Decisions cited:
T 0037/85

Catchword:
-



Case Number: T 0811/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 27 April 2001

Appellant: ACTEL CORPORATION
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 3 March 1997
refusing European patent application
No. 91 306 176.8 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. B. Günzel

Summary of Facts and Submissions

I. European patent application No. 91 306 176.8 (Publication No. 0 469 728) was refused by a decision dated 3 March 1997 of the examining division on the ground that the subject-matter of the claims lacked an inventive step having regard to the prior art documents

D1: US-A-4 758 745,

D2: Proceedings of the IEEE 1985 Custom Integrated Circuits Conference, Portland, Oregon, 20 to 23 May 1985, pages 12 and 13, and

D3: Patent Abstracts of Japan, vol. 13, no. 254 (E-772) (3602), 13 June 1989 & JP-A-01 053 430.

II. Claim 1 forming the basis of the decision is the only independent claim and reads as follows:

"1. An integrated circuit array architecture user-configurable after manufacture including:

a two-dimensional array of functional circuit modules (12) disposed within a semiconductor substrate, said functional circuit modules being arranged in an array of rows and columns;

a first interconnect layer disposed above and insulated from said semiconductor substrate, said first interconnect layer including a plurality of first conductors (16) which make connections internal to ones of said functional circuits;

a second interconnect layer disposed above and insulated from said first interconnect layer, said second interconnect layer including a plurality of second conductors (40-62) forming segmented tracks and running in a first direction;

a third interconnect layer disposed above and insulated from the second interconnect layer including a plurality of segmented tracks forming third conductors (120-140) running in a second direction, some of the segments of the third conductors forming intersections with ones of the segments of the second conductors (40-62) in said second interconnect layer;

a plurality of first user-configurable interconnect elements (290-308) placed directly between the second and third interconnect layers at the intersections of selected segments of the segmented conductors in the second and third interconnect layers;

a plurality of second user-configurable interconnect elements (262-286) located between adjacent segments of the segmented conductors in both said second and third interconnect layers; and

series pass transistors (200-260) located in said semiconductor substrate between the functional circuit modules, said series pass transistors being connected between adjacent segments in both said second and third interconnect layers, across respective ones of said second user-configurable interconnect elements (262-286);

wherein said second direction is substantially orthogonal to said first direction, said pluralities of second and third conductors run directly on top of said

functional circuit modules and said second and third interconnect layers are used to interconnect functional circuit modules."

III. The examining division reasoned essentially as follows:

The subject-matter of claim 1 is new. It differs from the explicit teaching of document D1 only in that

- (a) the first interconnect layer is provided between and isolated from the semiconductor substrate and from the interconnect layers including the segmented tracks, this first interconnect layer including conductors making interconnections internal to the functional circuit modules;
- (b) the segmented conductors run directly on top of the functional circuit modules; and
- (c) the first user-configurable interconnect elements are placed directly between the interconnect layers containing the segmented tracks at the intersections of selected segments.

These distinguishing features relate to different aspects of the objective problem addressed by the application in suit.

The distinguishing feature (a) avoids interference between the interconnections within the circuit modules and the conductors in the user-configurable interconnect layers. In the design and layout of multilevel metallisation structure of an integrated circuit, however, it was a routine practice to employ the lowermost interconnect layer for the internal connections within the functional circuit modules and to separate the lowermost interconnect layer from the user-configurable interconnect layers.

The aspect behind distinguishing feature (b) is the desire to gain space in the semiconductor substrate for additional functional circuits or to reduce the overall size of the circuit array architecture and thus to reduce the average interconnect lengths.

Concerning said distinguishing feature (b), document D2 (see the chapter "Introduction" on page 12) teaches to reduce the semiconductor substrate area occupied by a circuit array by the use of a circuit architecture without dedicated wiring channels by arranging the conductors of the interconnect layers above the functional circuits. A similar teaching is given by document D3. Since documents D1 to D3 refer to the same technical field of integrated circuit architecture, for the skilled person, no inventive skill is necessary to adopt the deletion of dedicated wiring channels known from documents D2 and D3 to the user-configurable array architecture as known from document D1.

The applicant has argued that the skilled person concerned with user-configurable circuit array architecture of document D1 would not regard the teaching of documents D2 and D3 to be relevant, since the latter documents are concerned with mask-configurable circuit arrays which are not configurable by the end user after the manufacture. This argument is not found convincing, since the skilled person is presumed to be aware of the entire technical field of circuit architecture and would therefore utilize different circuit arrays referred to in documents D2 and D3.

As regards feature (c), in Figure 7(A) of document D1 user-configurable element (46) providing a configurable interconnection between intersecting segments of two adjacent interconnect layers is provided in the immediate vicinity of the intersection (64) of the two

interconnect layers. For a skilled person, it would be obvious to place the element (46) at the intersection so as to avoid unnecessary increase in the wiring resistance and to save the space.

IV. The applicant lodged an appeal against this decision on 30 April 1997, paying the appeal fee on the same day and filing the statement of grounds of appeal on 9 July 1997.

The appellant (applicant) requested that the decision under appeal be set aside and that a patent be granted on the basis of the patent application documents forming the basis of the decision, i.e.,

Description:

Pages 1 to 5, 7 and 9 to 11 as filed;
Pages 6 and 8 as filed with applicant's letter dated 2 December 1994,

Claims:

Nos. 1 and 2 as filed during the oral proceedings of 28 January 1997 before the examining division, and

Drawings:

Sheets 1/3 to 3/3 as filed with applicant's letter dated 2 October 1991,

Moreover, he requested oral proceedings auxiliarily.

V. The appellant provided essentially the following arguments in support of his request:

The subject-matter of claim 1 differs from the prior art known from document D1 in

- the provision of three separate wiring layers for, respectively, internal wiring within circuit modules and two wiring layers for connections between circuit modules;
- the provision of interconnect elements between second and third layers of interconnect and within the second and third wiring layers;

and in that the conductors making connections between different functional circuit modules run over said functional circuit modules.

The problem addressed by the present invention consists in improving the density of circuit modules in an integrated circuit architecture user configurable after manufacture without reducing the flexibility of the interconnect structure; thus, the user is able to utilise all gates in a denser array. The distinguishing features enable to achieve this result.

The examining division has misconstrued the prior art. Documents D2 and D3 teach a channelless structure, the interconnections being moved from the channels separating the cells to the interior of the cells, where they run through the cells, amongst the internal connections in said cells, and not above the cells. There is no indication in the prior art about the other distinguishing features either.

For an invention to lack an inventive step, the specific combination of claimed features must be obvious (cf. the decision T 37/85, OJ EPO 1988, 086); this is not the case for the present invention, for which some of the plurality of distinguishing features are not disclosed in the prior art.

Therefore, the subject-matter of claim 1 involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.
2. The only issue in the present appeal is that of inventive step.
 - 2.1 An integrated circuit array architecture, user-configurable after manufacture, is known from document D1 (see in particular Figures 2a, 2b, 3 to 6, 7A, 7B and 8A and the corresponding text), which includes a two-dimensional array of functional circuit modules (20) disposed within a semiconductor substrate, said functional circuit modules being arranged in an array of rows and columns. The two interconnect layers (22, 24), which are orthogonal to each other, are insulated from the substrate and from each other and include a plurality of conductors in the form of segmented tracks having first user-configurable interconnect elements (46) between intersecting segments of the interconnect layers and second user-configurable interconnect elements (38A, 38B, 38C) between adjacent segments in both interconnect layers. Series-pass transistors are connected across respective ones of the second user-configurable elements.

Contrary to the prior art known from document D1, the subject-matter of claim 1 comprises:

- (a) a first interconnect layer provided between and isolated from the semiconductor substrate and from the interconnect layers including the segmented

tracks, this first interconnect layer including conductors making interconnections internal to the functional circuit modules;

- (b) the conductors of the second and third interconnect layers, which make connections between different functional circuit modules and which run on top of said functional circuit modules, and
- (c) the first user-configurable interconnect elements, which are placed directly between the interconnect layers containing the segmented tracks at the intersections of selected segments.

2.2 According to the present application (see page 1, the four last lines of the second paragraph; page 2, lines 24 to 33; see also page 3, lines 19 to 24), wherein document D1 is acknowledged, the present invention enhances the functional density of previously disclosed programmable interconnect architectures by placing the segmented routing tracks directly on top of the arrays of functional circuit modules, and the spacing between adjacent ones of the functional circuit modules need not include the spacing for dedicated routing channels as in the prior art; because the functional circuit modules in the array are spaced more closely together, shorter interconnect length may be used, thus improving the overall performance of the mapped applications.

Moreover, the appellant has argued that an object of the present invention is to obtain these improvements without however losing the functionality and flexibility of the known user-configurable architectures.

2.3 Indeed, document D2 (see in particular page 12, the title and the abstract) teaches that, in integrated circuit organized as standard cells, the wiring channels are not needed and that these connections between modules can be made by using wiring through the modules; this results in the integration degree of the cells being improved by a space equivalent to the wiring channels and in a significant reduction of the length of the interconnect length and thus in a reduction of the capacitance associated with these interconnects and therefore in a significant speed improvement.

Since this document relates to the architecture of integrated circuit arrays of functional circuit modules and since moreover it refers, for instance on page 12, right-hand column, second paragraph, to the user-configurable organization of such arrays, it is to be considered that the person skilled in the art of document D1, i.e. of integrated circuit array architecture which are user-configurable after manufacture, would have been aware of the developments in the related technical fields of standard cells design, i.e. of document D2, which could be useful for developments in his own technical field.

However, as already mentioned here above, according to document D2, the connections between modules can be made by using wiring through the modules, and there is no derivable indication that the interconnections between the functional circuit modules include conductors which run directly on top of said functional circuit modules, in particular above a first interconnect layer for connections internal to the cells. Thus, only part of the feature (b) distinguishing claim 1 from the arrangement of document D1 is derivable from document D2. There is no

indication either that these interconnections between the functional circuit modules include the specific arrangement of the second and third interconnect layers, the third interconnect layer being disposed above the second interconnect layer and being insulated therefrom, as in present claim 1.

There is also no information about any specific first interconnect layer, disposed above and insulated from the semiconductor substrate, said first interconnect layer including a plurality of first conductors which make connections internal to ones of the functional circuit modules.

In this respect, it is to be noted that document D2 (see the title and the abstract) concerns in particular a channelless architecture of circuits based on CMOS standard cells, whereby the resultant circuits are developed using a fully automated design system, and there is no indication that this fully automated design system is prepared for forming the specific arrangement of three layers of conductors of present claim 1.

Moreover, there is no information in document D2 about first user-configurable interconnect elements placed directly between the second and third interconnect layers at the intersections of selected segments of the segmented conductors in the second and third interconnect layers, as in present claim 1.

- 2.4 Document D3 (see the abstract with the shown Figure) provides a teaching similar to that of document D2. Since this document also relates to integrated circuit arrays of functional circuit modules and thus can contain information which can be useful for

developments in the art of integrated circuit array architecture user-configurable after manufacture, the person skilled in this particular art would be aware of it.

However, according to document D3, the connections between modules are made, at least for the above-mentioned first layer of metallic wirings (58, 63, 77, 82 and 91), by using wiring through the interior of each cell, and there is no derivable indication that the interconnections between the functional circuit modules include conductors which run directly on top of said functional circuit modules. Thus, here again, only part of the feature (b) distinguishing claim 1 from the arrangement of document D1 is derivable from document D3. There is no indication either that these interconnections between the functional circuit modules include the specific arrangement of the second and third interconnect layers, the third interconnect layer being disposed above the second interconnect layer and being insulated therefrom, as in present claim 1.

It is also to be noted that there is no information in document D3 about first user-configurable interconnect elements placed directly between two superposed interconnect layers at the intersections of selected segments of the segmented conductors, as in present claim 1.

- 2.5 Since as set forth here above the same specific features (a), (c) and part of (b) distinguishing claim 1 from the arrangement known from document D1, are also missing in each of the documents D2 and D3, the combination of the teachings of these three documents does not lead in a straightforward way to the subject-matter of present claim 1.

2.6 In the decision under appeal, it is argued that the three features (a), (b) and (c) distinguishing present claim 1 from the teaching of document D1 and which are not disclosed in documents D2 and D3 correspond to three partial problems which are each indicated, at least in part, at least in one of said prior art documents; the skilled person would find in the teaching of those documents the advantageous arrangements which are the solutions to these problems.

However, this reasoning is not convincing for the following reasons:

As argued in the statement setting out the grounds of appeal (see paragraphs 9, 10 and 13), the problem to be addressed by the present invention can be stated as to improve the density of circuit modules in an integrated circuit architecture user configurable after manufacture without reducing the flexibility of the interconnect structure, i.e., wherein all gates in the denser array can be utilised by the user.

Indeed, it is credible that the above-mentioned distinguishing features (a), (b) and (c) cooperate together to solve the problem, in particular by taking advantage of the specific location of the different interconnect layers and of the first user-configurable elements, so that an increase in the density of the functional circuit modules can be obtained without any sacrifice in flexibility of the interconnect structure.

As convincingly argued by the appellant by referring to the above-mentioned decision T 37/85 (see in particular point 4.5 of the reasons), for an invention to lack an inventive step, the specific combination of claimed features must be obvious; this is not the case for the

present invention, for which the distinguishing features in combination form a specific arrangement of the interconnect layers and this arrangement was not rendered obvious by the documents D1 to D3.

- 2.7 Therefore, for a skilled person, the subject-matter of present claim 1 is not obvious having regard to the state of the art and, thus, it involves an inventive step in the sense of Article 56 EPC.
- 2.8 Consequently, the claim is patentable and a patent can be granted on this basis (Article 52(1) and 97(2) EPC).
3. Therefore, the oral proceedings requested auxiliarily by the appellant are not necessary.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the examining division with the order to grant a patent on the basis of the following patent application documents:

Description:

Pages 1 to 5, 7 and 9 to 11 as filed;
Pages 6 and 8 as filed with applicant's letter dated 2 December 1994;.

Claims:


Nos. 1 and 2 as filed during the oral proceedings of 28 January 1997 before the examining division;


Drawings:

Sheets 1/3 to 3/3 as filed with applicant's letter dated 2 October 1991.

The Registrar:

The Chairman:


L. Martinuzzi


R. K. Shukla

MCH