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D E C I S I O N
of 21 March 2002

Case Number: T 0725/97 - 3.4.3

Application Number: 93112884.7

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Language of the proceedings: EN

Title of invention:
Semiconductor integrated circuit device and method of manufacturing the same

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
Shallow juction transistor/TOSHIBA

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes - after amendments)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0725/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 21 March 2002

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 27 January 1997 refusing European patent application No. 93 112 884.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. L. Eliasson
Members: V. L. P. Frank
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 93 112 884.7 was refused by the decision of the examining division dated 27 January 1997. The ground for the refusal was that the subject-matter of claim 1 according to the request filed during the oral proceedings held on 19 September 1996 did not involve an inventive step (Article 56 EPC) having regard to a combination of the prior art documents

D1: 1991 Symposium on VLSI Technology, May 28 to 30, 1991, pages 109 to 110, and

D4: IEEE Journal of Solid-State Circuits, volume 24, No. 5, 1989, pages 1170 to 1175

In the decision under appeal the examining division further observed that the subject-matter of the dependent device claims 2 to 4, independent method claim 5 and use claim 6 did also not involve an inventive step having regard to these documents and the general knowledge of the skilled person.

II. The wording of independent claim 1 of the request on which the decision of the examining division was based is as follows:

"1. A semiconductor integrated circuit device comprising:

- a semiconductor substrate (10) of a first conductive type;

- a first well region (11) of a second conductive

type formed on a second well region (12) of the first conductive type formed on said semiconductor substrate;

- a third well region (13) of the first conductive type formed on a fourth well region (14) of the second conductive type formed on said semiconductor substrate and adjoined to said first well region (11);

- field oxide isolation films (7) provided on the surface of said first and third well regions (11, 13) and enclosing activation regions of the device;

- a first MOS field effect transistor (30, 40, 50) of the first conductive type formed in said first well region (11) and having a first gate electrode (50) formed on a first gate isolation film (40);

- a second MOS field effect transistor (3, 4, 5) of the second conductive type formed in said third well region (13) and having a second gate electrode (5) formed on a second gate isolation film (4);

- means (15, 16) formed on said first and third well regions (11, 13), respectively, for applying bias voltages;

- wherein the depth of said first well region (11) under said first gate electrode (50) of said first MOS field effect transistor from said gate isolation film (40) is equal or less than 0.5 µm;

- wherein the depth of said third well region (13) under said second gate electrode (5) of said second MOS field effect transistor from said gate isolation film (4) is equal or less 0.5 µm;

- wherein said first well region (11) having a part equal or less than 0.5 µm at the respective activation region, which is enclosed by said field oxides isolation films (7), has a deeper part as a channel stopper under the field oxide isolation films (7); and

- wherein said third well region (13) having a part equal or less than 0.5 µm at the respective activation region, which is enclosed by said field oxide isolation films (7), has a deeper part as a channel stopper under the field oxide isolation films (7)."

III. The appellant (applicant) lodged an appeal on 27 March 1997, and paid the appeal fee on the same date. The statement setting out the grounds of appeal was filed on 27 May 1997.

IV. In a communication annexed to the summons to oral proceedings, the board expressed its preliminary view that the subject-matter of claims 1, 2, 4 and 5 did not appear to involve an inventive step over the disclosure of document D1 and the general knowledge of the skilled person.

V. At the oral proceedings which took place on 21 March 2002, the appellant filed a new set of claims 1 to 5 and amended pages of the description, requesting that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 5 filed during the oral proceedings;

Description: pages 1, 2, 10, 13 to 19 as originally filed;

pages 3, (5 and 6 deleted), 7 filed with the letter of 2 May 1995;
page 4 filed with the letter of 15 January 1996;
pages 8, 9, 11, 12, 22, 23 filed with the letter of 19 August 1996;
pages 4a, 20, 21 filed during the oral proceedings;

Drawings: Sheets 1/6 to 6/6 filed with the letter of 19 August 1996.

The independent device claim 1 according to this request differs from claim 1 on which the decision of the examining division was based in that its fourth paragraph reads as follows (emphasis added by the Board):

"- a third well region (13) of the first conductive type formed on a fourth well region (14) of the second conductive type formed on said semiconductor substrate, **said fourth well region (14) being electrically connected to said first well region (11) by contact therewith**;"

The independent method claim 4 according to this request reads as follows (emphasis added by the Board):

"4. A method of manufacturing a semiconductor integrated circuit, comprising the steps of:

forming a second well region (12) of a first conductive type on a semiconductor substrate (10) of the first conductive type in a region where a first MOS transistor is to be formed;

forming a fourth well region (14) of a second conductive type on the semiconductor substrate (10) adjoining to the second well region (12) and where a second MOS transistor is to be formed;

forming a first well region (11) of the second conductive type in a region in the second well region (12), where a source, a drain and a channel of said first MOS field effect transistor are to be formed;

forming a third well region (13) of the first conductive type in a region in the fourth well region (14), where a source, a drain and a channel of said second MOS field effect transistor are to be formed;

forming a first MOS field effect transistor (30, 40, 50) of the first conductive type in said first well region (11) and having a first gate electrode (50) formed on a first gate insulating film (5); and

forming a second MOS field effect transistor (3, 4, 5) of the second conductive type in said third well region (13) and having a second gate electrode (5) formed on a second gate insulating film (4);

forming isolation films on the surface of said first (11) and third (13) well regions;

forming means (15, 16) for applying bias voltages to the first (11) and third (13) well regions, respectively;

determining a depth of said first well region under the

first gate electrode of said first MOS field effect transistor from a surface of said semiconductor substrate to be such that a depletion layer extending from an interface between the first gate insulating film and said first well region in response to a gate voltage applied to the first gate electrode can be connected to a depletion layer formed at an interface between said first well region and the second well region and further determining a depth of said third well region under the second gate electrode of said second MOS field effect transistor from the surface of said semiconductor substrate to be such that a depletion layer extending from an interface between the second gate insulating film and said third well region in response to a gate voltage applied to said second gate electrode can be connected to a depletion layer formed at an interface between said third well region and said fourth well region;

characterized in that

said method further comprises the steps of:

electrically connecting said fourth well region (14) to said first well region (11) **by contact therewith**;

forming said third well region to have a shallower part at a first element forming region which is defined by said isolation films and a deeper part as a channel stopper under the isolation films;

forming said first well region (11) to have a shallower part at a second element forming region which is defined by said isolation films and a deeper part as a channel stopper under the isolation films; and

forming the second well region (12) of the first conductivity type to enclose sides and a lower surface of said first well region (11)."

VI. In the decision under appeal the examining division argued essentially as follows:

The semiconductor integrated circuit according to claim 1 differs from the NMOS shallow junction well transistor (SJET) disclosed in document D1 in that the former comprises a second PMOS SJET of the opposite conductivity type. The objective problem was therefore seen in applying the particular structure of the single SJET disclosed in this document to a CMOS circuit. However, it would have been obvious for a skilled person to apply the known transistor's structure to the CMOS DRAM triple-well structure disclosed in document D4. In particular, as in claim 1 the second well region (12) cannot be distinguished from the substrate (10), since both have the same conductivity type and no other differentiating features are specified in the claim. For interpreting the scope of the claim, the second well region can therefore be regarded as being part of the substrate and the claimed structure is thus equivalent to a triple-well structure.

Moreover, the claimed feature that the fourth well region 14 is adjoined to the first well region 11 would also be achieved by the combination of documents D1 and D4, since in document D4 the P-well 2 and the P-well 1 are adjoined to each other.

VII. The appellant argued essentially as follows:

(i) The examining division misinterpreted document D4, since the P-well (P-well 1) of the PMOS transistor is used for isolating the N-well from the n-type substrate. However, an isolation well is not required for the NMOS transistor. As acknowledged by the examining division, the combination of documents D1 and D4 would produce a triple-well structure and not the four-well structure claimed.

(ii) The conclusion of the examining division that the second well cannot be differentiated from the substrate is incorrect. In this context, reference was made to Article 69 EPC according to which the description and drawings shall be used to interpret the claims. A skilled person would immediately understand that the term "well region" means a region defined by an electrical potential well, regardless of the conductivity type of the regions involved.

(iii) The gist of the invention is to bias the buried fourth well without requiring a specific electric contact at the surface of the integrated circuit. This is achieved by providing a buried contact between the first and the fourth well so that both are polarized by the bias voltage applied to the first well.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments

The amendments made to claims 1 and 4 clarify the fact that it is the first well region 11 which adjoins and is in electrical contact with the fourth well region 14. This amendment is based on Figure 1 of the application in suit and is, furthermore, consistently described as a feature of the invention (cf. column 7, lines 15 to 17; column 8, lines 6 to 9; column 11, lines 8 to 13; column 14, lines 26 to 29; column 16, lines 47 to 51 of the published application).

The board is therefore satisfied that the application complies with Articles 84 and 123(2) EPC.

3. Inventive step

The only remaining issue in this appeal is that of inventive step.

3.1 It is common ground that document D1 represents the closest prior art.

This document discloses a shallow junction well transistor (SJET) structure. In this structure a shallow p-type channel region, 0.15 µm deep, is implanted in a n-well which is in turn formed in a n-type substrate. The transistor is further completed by a gate oxide, a n^+ polysilicon gate electrode and n^+ source/drain regions (cf. Figure 1 and page 109, "Experimental procedure"). The p-type channel region of this transistor corresponds, using the wording of claim 1, to the first well region 11 and the underlying n-well to the second well region 12.

Field oxide isolation films and channel stopper regions are formed on both sides of the transistor. An

electrode V_b for biasing the n-well is formed at the back of the substrate, and an electrode V_w for biasing the p-well is formed at the side of the field oxide isolation film opposite to the side on which the transistor is formed (cf. D1, Figure 1 and 2).

Since the p-well is very shallow, the depletion layer width of the p-well/n-well junction extends to the channel depletion layer, reducing its capacitance. It is conjectured in this document, that the disclosed transistor would be a promising structure for future VLSIs due to its improved properties (cf. page 109, right-hand column, last sentence).

3.2 The semiconductor device according to claim 1 differs from the transistor known from document D1 essentially in that

(i) a second transistor of the opposite conductivity type (eg a PMOS FET) is formed adjacent to the first transistor (eg a NMOS FET), and in that

(ii) the first transistor's channel well (ie the first well region 11) is in contact with and electrically connected to the second transistor's well (ie the fourth well region 14) underlying the second transistor's channel well (ie the third well region 13).

3.3 In view of the above mentioned differences the board considers that the problem addressed by the invention is the provision of a CMOS (complementary metal oxide structure) circuit which benefits of the improved properties of the transistor disclosed in document D1 and wherein the buried well, having the opposite

conductivity type as the substrate and in which the channel well is formed, can be easily biased.

According to the application in suit, the provision of a special electrode (cf. the application in suit Figure 9, V_{bb}) for biasing the buried well region underlying the channel well requires that this region extends up to an open area of the semiconductor device. However, this is hard to achieve, since the well regions must be formed as shallow as possible for miniaturization and, therefore, such an open area cannot be easily obtained (cf. ibid, column 2, line 45 to column 3, line 6). By electrically contacting the first and fourth well regions 11 and 14, a special electrode for biasing the buried fourth well region is not required, since this is accomplished by the biasing electrode V_{pw} of the first well region (cf. ibid, Figure 1).

In consequence, the board is satisfied that the objective problem stated above is solved by the claimed semiconductor integrated circuit.

3.4 It has been argued by the examining division that the feature mentioned under point 3.2(i) is the result of using the structure of the transistor known from document D1 in a CMOS circuit. No inventive step could be recognized in this.

The board concurs with this finding and the appellant has not contested it.

3.5 The examining division further argued that feature 3.2(ii) was obvious for a skilled person having regard to the semiconductor integrated circuit

disclosed in document D4.

3.5.1 This document discloses a DRAM triple-well structure in which a CMOS circuit is formed by a pair of conventional NMOS/PMOS transistors (cf. D4, Figure 1). The NMOS transistor is formed within a p-type well (P-well 2) and the PMOS transistor within a n-type well (N-well). A further p-type well (P-well 1, which will be called the 'isolating p-well' in the following) is interposed between the N-well and the n-type substrate to electrically isolate the N-well from the substrate which is biased at an external voltage V_{ext}. This document states that the disclosed structure has the important technical advantage of making possible the optimum choice of bias potentials for all the p- and n-wells (cf. D4, page 1170, right-hand column, penultimate paragraph).

In this CMOS structure the p-well (P-well 2) forming the channel of the NMOS transistor and the isolating p-well are adjacent to each other and in electrical contact (cf. Figure 1). However, both p-wells have each a separate bias electrode (V_{ss}).

3.5.2 The examining division argued that the replacement of the transistors used in the circuit of document D4 by the shallow junction transistor disclosed in document D1 would result in a CMOS structure in which an electrical contact between the first and the fourth well, according to the wording of claim 1, would be achieved, since an electrical contact between these regions is already present in the circuit of document D4.

3.5.3 The board does not agree with this conclusion, since

the electric contact between both p-wells is shown in document D4 only in Figure 1 without any further reference to this feature in the text. The fact that both p-wells are in electrical contact with each other does not serve the purpose of biasing the isolating p-well by using the bias electrode of the p-channel, since the isolating p-well has its own bias electrode (cf. D4, page 1170, right-hand column, last paragraph).

According to the established case law of the boards of appeal, not only the structure of a feature, but also its technical function has to be derivable form a disclosure based solely on a drawing (cf. Case Law of the Boards of Appeal, 4th edition 2001, page 59, I.C.2.6, "Taking drawings into account"). In the present situation, however, the fact that both p-wells are adjacent to each other has not a directly derivable technical function that a skilled person would recognize as solving the problem addressed by the application in suit.

The board is for these reasons of the opinion that a skilled person, by replacing both MOS transistors in the device of document D4 with the shallow junction transistor known from document D1, would not arrive at the subject-matter of claim 1, since the replacement of one transistor type with the other type would result in a device having two shallow junction transistors of opposite conductivity type arranged side by side. In such an arrangement, however, the p-channel region of one transistor corresponding to the "first well" in claim 1 and the isolation p-well of the other transistor corresponding to the "fourth well" are neither "adjacent to" nor "in electric contact with each other", as specified in claim 1.

3.6 A similar reasoning applies to the subject-matter of method claim 4, since it also requires that the first and fourth well regions be in electrical contact to each other.

3.7 For the foregoing reasons, in the board's judgement, the subject-matters of claims 1 and 4 involve an inventive step in the sense of Article 56 EPC.

Dependent claims 2 to 3 and 5 concern further particular embodiments of the invention and are patentable for the same reasons.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent in the following version:

Description:
Pages 1, 2, 10, 13 to 19 as originally filed;
Pages 3, (5 and 6 deleted), 7 filed with the letter of 2 May 1995;
Page 4 filed with the letter of 15 January 1996;
Pages 8, 9, 11, 12, 22, 23 filed with the letter of 19 August 1996;
Pages 4a, 20, 21 received during the oral proceedings of 21 March 2002;

Claims:
No. 1 to 5 received during the oral proceedings of 21 March 2002;

Drawings:
Sheets 1/6 to 6/6 filed with the letter of 19 August 1996.

The Registrar: The Chairman:

D. Spigarelli G. L. Eliasson