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D E C I S I O N
of 10 July 2001

Case Number: T 0703/97 - 3.4.3

Application Number: 93110092.9

Publication Number: 0576001

IPC: H01L 29/06

Language of the proceedings: EN

Title of invention:
Power semiconductor integrated circuit device with uniform electric field distribution

Applicant:
Kabushiki Kaisha Toshiba

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Main request: inventive step (no - obvious option)"
"Determination of the objective technical problem"
"Auxiliary request - inventive step (yes)"

Decisions cited:
-

Catchword:
-

Case Number: T 0703/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 10 July 2001

Appellant: Kabushiki Kaisha Toshiba
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 29 January 1997 refusing European patent application No. 93 110 092.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. B. Günzel

Summary of Facts and Submissions

I. The European patent application No. 93 110 092.9 (publication No. 0 576 001) was refused by a decision of the examining division dated 29 January 1997 on the ground that it lacked an inventive step having regard to the prior art documents

D1: US-A-4 157 563,

D2: WO-A-85/03 167, and

D5: US-A-5 086 332.

Claim 1 of the main request forming the basis of the decision under appeal had the following text (subdivided into paragraphs (a) to (g) by the Board for facilitating discussion):

"1. A lateral power semiconductor integrated circuit device comprising

a) a semiconductor substrate (11) of a first conductivity type,

b) a first semiconductor region (12) of the first or, in case the lateral power semiconductor integrated circuit device is a DMOSFET, a second conductivity type provided in the semiconductor substrate (11),

c) a second semiconductor region (13) of the second conductivity type provided in the semiconductor substrate (11) spaced apart from the first semiconductor region (12),

d) an insulating film (14) provided on the semiconductor substrate (11) and covering at least partly the first and second semiconductor regions (12, 13),

e) a wiring layer (15) provided on the insulating film (14), connected to one of the first and second semiconductor regions (12, 13) and passing over the other of the first and second semiconductor regions (12, 13), and

f) a film resistor (17) formed in the insulating film (14), the film resistor (17) having a first end connected to the first semiconductor region (12) and having a second end which is either connected to the second semiconductor region (13) or, in case the lateral power semiconductor integrated circuit device is a DMOSFET, is set at a potential which has a potential difference of not more than several volts with respect to the second semiconductor region (13),

g) wherein the film resistor (17) is disposed above the semiconductor substrate (11) and is crossed by the wiring layer (15) at least once."

Claim 1 of the auxiliary request forming the basis of the decision essentially differed from claim 1 of the main request in that it further comprised the following features:

(g1) and wherein the lateral power semiconductor integrated circuit device is adapted to maintain a high potential difference in the order of several hundred volts between the first and second semiconductor regions (12, 13),

(g2) and between the wiring layer (15) and that one of the first and second semiconductor regions (12, 13) over which the wiring layer (15) passes.

II. In the decision, the examining division reasoned essentially as follows:

Main request

First alternative

The subject-matter of this claimed device differs from that of Figure 1 of document D2 in that, in claim 1, the wiring layer passes over the other of the first and second semiconductor regions and in that the film resistor is crossed by the wiring layer at least once.

Since in document D2 the high breakdown voltage device is part of an integrated circuit, it is an obvious option for the skilled person to form the wiring layers only over the device (10) and not over other parts of the chip in order not to decrease the integration density.

Similarly claim 1 is distinguished from the device known from Figure 6 of document D1 by the same features mentioned above. The objective problem solved by these differences may be seen as leading wiring layers from the semiconductor regions to the external circuitry, and this is a generally known problem. In any case, since the structure shown in Figure 6 of the document is of concentric shape, the skilled person would automatically arrive at the structure of claim 1.

Second alternative (DMOSFET)

In the claimed device, the wiring layer passes over the second semiconductor region and the film resistor is crossed by the wiring layer at least once, and this constitutes in substance the only differences with respect to the DMOSFET known from Figure 30 of document D5.

However, in order to avoid unnecessary increase of device size, it is again obvious to the skilled person to form the wiring layer only over the device and not over other parts of the substrate where no elements of the DMOSFET are formed.

Therefore, the subject-matter of claim 1 of the main request lacks an inventive step.

Auxiliary request

The additional features (g1) and (g2) *per se* are known from document D1; indeed, this known device is for withstanding reverse voltages of 1000 volts, so that it is clear that this device is adapted to maintain this voltage difference between the first and the second semiconductor regions over which the wiring layer passes.

Therefore, the subject-matter of claim 1 of the auxiliary request also lacks an inventive step.

III. The applicant lodged an appeal against this decision on 14 March 1997 paying the appeal fee on the same day. The statement setting out the grounds of appeal was filed on 9 June 1997.

IV. With letter dated 11 May 2001 the appellant (applicant) filed a new set of claims and a new complete description in preparation for the oral proceedings, forming the basis of his **main request**.

Also, during the oral proceedings of 10 July 2001, the appellant filed a new text of the description and a set of claims forming the basis of an **auxiliary request**.

The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the patent application documents according to the following main or auxiliary request:

Main request

Description: Pages 1a, 1b, 1c, 1d, 1e and 2 to 14 filed with letter of 11 May 2001;

Claims: Nos. 1 to 17 filed with letter of 11 May 2001;

Drawings: Sheets 1/8 to 8/8, as filed;

Auxiliary request

Description: Pages 1a, 1b, 1c, 1d, 1e and 2 to 14 filed during the oral proceedings of 10 July 2001;

Claims: Nos. 1 to 10 filed during the oral proceedings of 10 July 2001;

Drawings: Sheets 1/8 to 8/8, as filed.

V. Claim 1 of the main request has the following wording:

"1. A lateral power semiconductor integrated circuit device comprising

a) a semiconductor substrate (11) of a first conductivity type,

b) a first semiconductor region (12) of the first conductivity type provided in the semiconductor substrate (11),

c) a second semiconductor region (13) of a second conductivity type provided in the semiconductor substrate (11) spaced apart from the first semiconductor region (12),

d) an insulating film (14) provided on the semiconductor substrate (11) and covering at least partly the first and second semiconductor regions (12, 13),

e) a wiring layer (15) provided on the insulating film (14), connected to one of the first and second semiconductor regions (12, 13) and passing over the other of the first and second semiconductor regions (12, 13), and

f) a film resistor (17) formed in the insulating film (14), the film resistor (17) having a first end connected to the first semiconductor region (12) and having a second end connected to the second semiconductor region (13),

g) wherein the film resistor (17) is disposed above the

semiconductor substrate (11) and is crossed by the wiring layer (15) at least once."

Claims 2 and 3 of this set are independent claims directed to a lateral power semiconductor integrated circuit device formed as DMOSFET and as an IGBT, respectively. In particular, claim 3 differs from claim 1 essentially in that,

the first semiconductor region (61) is of the second conductivity type (feature (b)),

and in that

the second end of the film resistor (17) formed in the insulating film (14) is connected either to the gate electrode (G) or to the emitter electrode (E) of the IGBT (feature f).

Claim 1 of the auxiliary request comprises features corresponding to the DMOSFET illustrated by Figures 4A and 4B of the application in suit and it reads as follows:

"1. A lateral power semiconductor integrated circuit device formed as a DMOSFET comprising:

a) a semiconductor substrate (11) of a first conductivity type (N),

b) a first semiconductor region (12) of the first conductivity type provided in the semiconductor substrate (11),

c) a second semiconductor region (13) of a second

conductivity type (P) provided in the semiconductor substrate (11) spaced apart from the first semiconductor region (12),

d) a third semiconductor region (41) of the first conductivity type (N) provided in the second semiconductor region (13),

e) an insulating film (14) provided on the semiconductor substrate (11) and covering at least partly the first and second semiconductor regions (12, 13),

f) a wiring layer (15) provided on the insulating film (14), connected to the first semiconductor region (12) and passing over the second semiconductor region (13), and

g) a film resistor (17) formed in the insulating film (14), the film resistor (17) having a first end connected to the first semiconductor region (12) and having a second end overlying the second semiconductor region (13) which operates as the gate electrode (17') of the DMOSFET,

h) wherein the film resistor (17) is disposed above the semiconductor substrate (11) and is crossed by the wiring layer (15) at least once."

Claims 2 to 10 are dependent on claim 1.

VI. The appellant submitted the following arguments in support of his requests:

Main request

The problem and solution approach as applied in the decision under appeal is not correct since it relies on document D1 as the closest prior art. Document D1 is concerned with a planar semiconductor device having semiconductor regions arranged in the vertical direction. The device according to the present invention however relates to a totally different type of device, i.e., a lateral device, so that the skilled person concerned with a lateral semiconductor device would not start from a planar semiconductor device of document D1. Also, the problem addressed by the present invention arises due to a high voltage wiring layer passing over a semiconductor region, and is not to provide a lead wire connection to a semiconductor region as stated in the decision under appeal.

In view of the device shown in Figure 1 of document D2 wherein each of the first and second semiconductor regions (14, 16) and of their respective electrodes (20, 22) is near one extremity of the resistor (26), the simplest way of connecting each of the electrodes (20, 22) to the external circuitry is to form a wiring which passes over the respective extremity of the resistor and which thus does not pass over the other semiconductor region located at the opposite extremity of the resistor (26).

Therefore, starting from document D2, it is not obvious to the skilled person to arrive at the device of claim 1.

Auxiliary request

The DMOSFET device of claim 1 is based on the application as filed (see claims 1, 12 and 13 and the

embodiment illustrated by Figures 4 and 4A).

The closest prior art is represented by Figure 30 of document D5. Starting from this known device with a completely different structure, there is no indication for any modifications which would lead to the claimed device.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 Inventive step - Claim 1

2.1.1 Document D2 relates to a lateral power semiconductor integrated circuit device as the present invention, and is regarded as the closest prior art as contended by the appellant (cf. Figure 1 and the corresponding description). The device comprises:

(a) a semiconductor substrate (12) of a first conductivity type (P),

(b) a first semiconductor region (14) of the first conductivity type provided in the semiconductor substrate (12),

(c) a second semiconductor region (16) of a second conductivity type (N) provided in the semiconductor substrate (12) spaced apart from the first semiconductor region (14),

(d) an insulating film (24, 28) provided on the semiconductor substrate (12) and covering at least partly the first and second semiconductor regions (14, 16),

(f) a film resistor (26) formed in the insulating film (24), the film resistor (26) having a first end connected to the first semiconductor region (14) and having a second end connected to the second semiconductor region (16),

(g) wherein the film resistor (26) is disposed above the semiconductor substrate (12).

It is to be noted that electrodes (20) and (22) making contact with the first and second semiconductor regions (14, 16) respectively are shown in Figure 1; since connection to an external circuitry is necessary, it is directly and unambiguously derivable that

(e') a wiring layer is provided on the insulating film (24, 28), connected to one of the first and second semiconductor regions (14, 16).

Moreover, since in the structure shown in Figure 1 of document D2 the electrodes (20, 22) to these semiconductor regions (14, 16) are surrounded by a part of the film resistor (26), a connection from any of said two electrodes (20, 22) to the external circuitry can only take place over a part of the film resistor (26), so that

(g') the resistor (26) is crossed by the wiring layer (15) at least once.

However, there is no information in document D2 that the necessary wiring layer provided on the insulating film (24, 28) and connected to one of the first and second semiconductor regions (14, 16) passes over the other of the first and second semiconductor regions (16, 14).

2.1.2 In the high voltage semiconductor device of document D2, the film resistor shields the PN junction formed in the semiconductor substrate from the electric charges accumulated on the top surface of the insulating film and thereby prevents the reduction of the PN junction breakdown voltage (cf. page 1, lines 1 to 27). Thus, the problem of reduction of the PN junction breakdown voltage addressed in the application in suit is already solved in the closest prior art device in a manner as set out in the present invention as claimed in claim 1. According to the established case law of the boards of appeal, this problem therefore cannot be taken into consideration in the formulation of the objective technical problem addressed by the invention as claimed, as compared with the closest prior art, (cf. Case Law of the Boards of Appeal, Third Edition 1998, D 4.1, pages 114 and 115).

Thus, as stated in the decision under appeal, starting from the device of Figure 1 of document D2, the objective problem remaining to be solved is to complete the structure of the device shown by providing a wiring layer and thereby connecting the electrodes (20, 22) making contact to the first and second semiconductor region to the external connections of the chip.

It was argued by the appellant that, in view of the device shown in Figure 1 of document D2 wherein both the first and second semiconductor regions (14, 16) and their respective electrode (20, 22) are near one extremity of the resistor (26), the simplest way of connecting each of the electrodes (20, 22) would have been to form a wiring which passes over the respective extremity of the resistor and which thus does not pass over the other semiconductor region located at the opposite extremity of the resistor (26).

The Board accepts that this was one of the possibilities of arranging the wiring layers. However, as convincingly set forth in the decision under appeal, since the device of document D2 is an integrated device, it was also an obvious option for the skilled person to form the wiring layers only over the device (10) and not over other parts of the chip in order not to decrease the integrated density. Thus, since adopting this alternative option for the arrangement of the wiring is necessary in view of the circumstances for high density integrated devices, the skilled person would arrive in an obvious way at the device of claim 1 wherein the wiring layers cross the resistor at least once.

2.1.1.3 Therefore, the subject-matter of claim 1 lacks an inventive step in the sense of Article 56 EPC.

The appellant's main request is accordingly not allowable (Article 97(1) EPC).

3. *Auxiliary request*

3.1 Formal requirements

Claim 1 is the only independent claim of the set of claims of the auxiliary request. It corresponds to subject-matter resulting from the combination of claim 1 and dependent claims 12, 13 and 14 as well as to the embodiment illustrated by Figures 4A and 4B of the application as filed.

Dependent claims 2 to 10 define specific forms of the device and in particular of the film resistors and correspond essentially to dependent claims 2 to 8 and 13 of the application as filed.

The main further amendments in the application concern the adaptation of the description to the new claim 1 and in particular the statements, inter alia on page 6, that Figures 1 to 3A and 5 to 7B do not relate to embodiments of the invention but are useful for understanding the invention.

Therefore, the Board is satisfied that the European patent application has not been amended in such a way that it contains subject-matter extending beyond the content of the application as filed, and that, moreover, the claims are clear and supported by the description (Articles 123(2) and 84 EPC).

3.2 Novelty

The subject-matter of claim 1 of the auxiliary request is not comprised in the state of the art and is thus new in the sense of Article 54 EPC.

3.3 Inventive step

3.3.1 A planar power semiconductor integrated circuit device

formed as a DMOSFET is known from document D5 (see Figure 30 and column 16, lines 1 to 14; see also column 7, line 33 to column 9, line 36 and Figures 5, 6, 7A to 7G and 8); the device of Figure 30 comprises:

(a) a semiconductor substrate (110) of a first conductivity type (P);

(b) a first semiconductor region (140, 152) of the first conductivity type provided in the semiconductor substrate (110);

(c) a second semiconductor region (112, 114, 158) of a second conductivity type (N) provided in the semiconductor substrate (110) spaced apart from the first semiconductor region (140, 152);

(d) a third region (160);

(e) an insulating film (142, 164) provided on the semiconductor substrate (110) and covering at least partly the first and second semiconductor regions (140, 152; 112, 114, 158);

(f) a wiring layer (166) provided on the insulating film (142, 164); and

(g) a film resistor (118, 156) formed in the insulating film (142, 164), the film resistor (118, 156) having a first end (118) connected to a semiconductor region (112, 114, 158) and having a second end (156) overlying the spaced semiconductor region (140, 152) which operates as the gate electrode of the DMOSFET;

(h) wherein the film resistor (118, 156) is disposed above the semiconductor substrate (110).

3.3.1.1 However, in the known device, the third semiconductor region (160) is not of the same conductivity type as the substrate and it is not provided in the semiconductor region of the conductivity type opposite to that of the substrate, as in claim 1 (feature (d)), but said third region is of the conductivity type (N) opposite to that (P) of the substrate (110) and it is provided in a semiconductor region (140, 152) with the same conductivity type (P) as the substrate (110).

Moreover, the wiring layer (166) of the known device, provided on the insulating film (142, 164), is not connected to the semiconductor region having the same conductivity type as the substrate and does not pass over the spaced semiconductor region having the opposite conductivity type, as in claim 1 (feature (f)), but is connected to a semiconductor region having the conductivity type (N) opposite to that (P) of the substrate (110), and there is no indication about this wiring extending so as to pass over the other, spaced semiconductor region (140, 152).

It is also to be noted that the film resistor (118, 156) formed in the insulating film (142, 164) of the known device has a first end (118) which is not connected to the semiconductor region of the same conductivity type as the substrate, as in claim 1; moreover, the second end (156) of the film resistor (118, 156) which operates as the gate electrode of the known DMOSFET overlies a semiconductor region (140, 152), but this semiconductor region is not of a conductivity type opposite to that of the substrate

(110) (feature (g)).

It is further to be noted that there is no indication that in the known device the film resistor (118, 156) is crossed by the wiring layer (15) at least once, as in feature (g) of claim 1.

3.3.1.2 Thus, in the known DMOSFET device, the gate electrode overlies a semiconductor region of the same conductivity type (P) as the substrate, i.e., the gate overlies a semiconductor region which is of the same conductivity type as a part of the substrate separating the first and second semiconductor regions (140, 152; 112, 114, 158). Indeed, as also shown in Figure 30 of document D5, in the known DMOSFET, the substrate (110) forms a part of the channel region under the gate electrode (156). Therefore, the known DMOSFET is of a type different from that of claim 1, wherein the substrate separating the spaced first and second regions is of a conductivity type opposite to that of the second region on which the gate electrode is overlying (feature (g)).

3.3.1.3 It is to be noted that document D5 discloses a plurality of other devices, some of them being also lateral power semiconductor integrated circuit devices formed as DMOSFET comprising features which differ from those of the embodiment illustrated by Figure 30. However, in none of these other known embodiments can be derived a device as that of claim 1 wherein in particular the substrate separating the spaced first and second regions is of a conductivity type opposite to that of the second region on which the gate electrode is overlying (feature (g)) or wherein the wiring layer provided on the insulating film and

connected to the semiconductor region having the same conductivity type as the substrate passes over the spaced semiconductor region having the opposite conductivity type (feature (f)).

3.3.2 Document D1 (see in particular the embodiment illustrated by Figures 3 and 4) and document D2 (see in particular the embodiment illustrated by Figure 1) concern other power semiconductor integrated circuit devices comprising regions of opposite conductivity spaced apart at the surface of a semiconductor substrate, with means comprising a film resistor for improving the breakdown characteristics of the devices. However, contrary to the device of claim 1 of the auxiliary request and to the device of Figure 30 of document D5, in these other known devices, the film resistors for improving the breakdown characteristics of the devices, which are connected at one end to the semiconductor region of the same conductivity type as the substrate, are not operating at the other end as a gate separated from the substrate by an insulating layer, but are connected at the other end of the film resistor to the semiconductor region of the conductivity type opposite to that of the substrate. In any case, these other known devices are not lateral power semiconductor integrated circuit devices formed as DMOSFET.

It is also to be noted that, in documents D1 and D2, there is no indication about the wiring for said other known devices and thus no indication that the wiring layer provided on the insulating film and connected to the semiconductor region having the same conductivity type as the substrate passes over the spaced semiconductor region having the opposite conductivity

type (feature (f)).

3.3.3 Starting from the device of Figure 30 of document D5, an object of the invention defined in claim 1 of the auxiliary request can be seen in the aim of providing an alternative structure of a lateral power semiconductor integrated circuit device formed as a DMOSFET having high breakdown voltage.

However, as discussed above the presently claimed device is not obvious from the documents D1, D2 and D5 taken individually or from any combination thereof.

Therefore, in the Board's judgment, for the person skilled in the art, the subject-matter of claim 1 of the auxiliary request is not obvious having regard to the state of the art and, thus, it involves an inventive step in the sense of Article 56 EPC, and the claim is patentable in the sense of Article 52(1) EPC.

3.3.4 Consequently, a patent can be granted on this basis (Article 97(2) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of the following patent application documents:

Description: Pages 1a, 1b, 1c, 1d, 1e and 2 to 14 filed during the oral proceedings of 10 July 2001;

Claims: Nos. 1 to 10 filed during the oral proceedings of 10 July 2001;

Drawings: Sheets 1/8 to 8/8, as filed.

The Registrar: The Chairman:

L. Martinuzzi R. K. Shukla