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D E C I S I O N
of 8 June 2001

Case Number: T 0612/97 - 3.4.3

Application Number: 90308151.1

Publication Number: 0413451

IPC: H01L 23/498

Language of the proceedings: EN

Title of invention:
Packaging semiconductor chips

Applicant:
STMicroelectronics Limited

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 84, 56

Keyword:
"Main request"
"Clarity (yes - after amendments)"
"Inventive step (yes - after amendments)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0612/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 8 June 2001

Appellant: STMicroelectronics Limited
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 13 January 1997 refusing European patent application No. 90 308 151.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
B. Günzel

Summary of Facts and Submissions

I. European patent application No. 90 308 151.1 (publication No. 0 413 451) was refused by a decision of the examining division dated 13 January 1997 on the grounds of lack of clarity of claim 1 of the main, first, third and fourth auxiliary requests, and of lack of inventive step of the subject-matter of claim 1 of the second and fifth auxiliary requests having regard to, *inter alia*, the following prior art documents:

D1: US-A-3 780 352 and

D5: EP-A-0 198 194.

II. Claim 1 of the main request forming the basis of the above decision reads as follows:

"1. A semiconductor device (2) comprising at least one semiconductor chip (4), the or each semiconductor chip (4) having a plurality of chip bonding pads (36), a package (6, 14) which encloses the at least one semiconductor chip (4), a first level interconnect which extends externally of the package (6, 14) to provide a plurality of outer leads (12), and a second level interconnect comprising means (38) for electrically connecting the chip bonding pads (36) to selected contacts (30) on the first level interconnect, which contacts (30) overlie the at least one semiconductor chip (4), characterised in that the first level interconnect comprises a printed circuit (8) which overlies the at least one semiconductor chip (4) in the package (6, 14) and comprises a plurality of electroconductive tracks (20) disposed between two layers (24, 26) of insulating material, the plurality

of electroconductive tracks (20) extending between opposed rows of outer leads on respective opposed ends of the printed circuit (8), one of said two layers of insulating material (26) which is remote from the or each semiconductor chip (4) either having holes (28) therein which reveal the said contacts (30) which comprise bonding pads of the electroconductive tracks (20), or having a plurality of electro conductive vias (96) of the electroconductive tracks (92) extending therethrough to comprise the contacts (30), and the means for electrically connecting respectively comprises either a plurality of bonding wires (38) each of which connects a respective bonding pad (30) to a respective chip bonding pad (36) or an array of electroconductive leads (100) each of which connects a respective via (96) to a respective chip bonding pad (98)."

III. The examining division reasoned essentially as follows:

Main request

Claim 1 of the main request defines a semiconductor device in which a printed circuit having a first level interconnect electroconductive tracks formed between two layers of insulating material overlies at least one semiconductor chip which has a plurality of bonding pads. In one alternative arrangement in the claim, holes are formed in the insulating layer of the printed circuit which is remote from the chip in order to reveal contacts which comprise bonding pads of said tracks. For this alternative, moreover, a second level interconnect which interconnects the chip bonding pads to the bonding pads of the electroconductive tracks comprises bonding wires.

In the absence of any further information in claim 1 as to the extension of the printed circuit and the mutual arrangement of the bonding pads, and the printed circuit with the tracks and the bonding wires, the requirement of providing a printed circuit which overlies one chip is contradictory to the requirement of forming an interconnection by a bonding wire between chip bonding pad and a bonding pad on an electroconductive track which is accessible for the bonding wire only through a hole in the insulating layer on the side remote from the chip.

Moreover, even if one were to concede that the skilled person could readily imagine device structures with appropriate windows in or with a properly limited extension of the printed circuit so as not to overlie the chip bonding pads, it would still be by no means clear which other structures or arrangements would fall under the definition of the claim. This is all the more true as claim 1 only vaguely defines that the means for electrically connecting the chip bonding pads to those on the tracks "comprise" bonding wires, so that further electrically conductive structures may participate in the desired interconnection and it remains even unclear whether or not the bonding wires should directly interconnect the respective pads. Thus it remains unclear what exactly would fall under the scope of protection conferred by claim 1.

Therefore, claim 1 was not clear.

Moreover, claim 1 of the main request was lacking an inventive step having regard to the prior art documents D1 and D5.

Auxiliary requests

Claim 1 of the first, third and fourth auxiliary requests, respectively, fail to give any information as to how bonding wires could effect the desired interconnection between the chip bonding pads and contacts of the electroconductive pads exposed on the side remote from the chips. These requests, therefore, do not comply with Article 84 EPC.

IV. The applicant lodged an appeal against this decision on 12 March 1997, paying the appeal fee on the same day. The statement setting out the grounds of appeal was filed on 13 May 1997, together with a new main request and two auxiliary requests. Moreover, oral proceedings were requested if the main request was not accepted.

Claim 1 is the only independent claim of the set of claims of the **main request**, and it comprises, as compared to claim 1 of the main request forming the basis of the decision under appeal, the following three additional features in the second part of the claim:

- "**the second level interconnect is located above the first level interconnect,**" inserted directly after the words "characterised in that",

- "**extends over the said one layer of insulating material (26) and**" inserted between the terms "either a plurality of bonding wires (38) each of which" and "connects a respective bonding pad (30)", and

- "**extends over the said one layer of insulating**

material (94) and" inserted between the terms "or an array of electroconductive leads (100) each of which" and "connects a respective via (96) to a respective chip bonding pad (98).

V. With the official communication dated 3 April 2001, the Board of appeal informed the appellant that, taking into account the amendments provided by the appellant, his arguments concerning the clarity of claim 1 of the main request and the patentability of its subject-matter were considered as convincing and that the description required amendments for consistency with the new claims.

VI. With his letter dated 11 May 2001, the appellant filed new pages 1 and 3 of the description.

VII. As a main request, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of:

Description:
Pages 2, 6 to 9, 13 and 14 as filed;
Pages 5, 10 to 12, 15 and 16 as filed with applicant's letter of 30 September 1993;
Page 4 as filed with applicant's letter of 26 July 1995;
Pages 1 and 3 as filed with appellant's letter of 11 May 2001;

Claims:
Nos. 1 to 6 as filed with appellant's letter dated 13 May 1997 (main request);

Drawings:

Sheets 1/5 to 5/5 as filed with applicant's letter of 30 September 1993.

VIII. The appellant submitted the following arguments in support of his main request:

Clarity

Claim 1 now specifies that the second level interconnect is located above the first level interconnect and thus above the printed circuit (8), and that each of the bonding wires (38) of the plurality of bonding wires (38) of the second level interconnect extends over the one layer of insulating material (26) remote from the or each semiconductor chip.

Taking into account these added features for the first alternative, there is no ambiguity about the mutual arrangement of the chip bonding pads (36), the printed circuit (8) with the electroconductive tracks (20) and the bonding wires (38). In particular, the printed circuit (8) which overlies the at least one chip (4) can be such that an interconnection by a bonding wire (38) can be formed between a chip bonding pad (36) on the chip and a bonding pad (30) on an electroconductive track (20), said latter pad being accessible for the bonding wire (38) running over both the chip (4) and said insulating layer. Thus, there is no contradiction in the claim between on the one hand requiring the printed circuit to overlie the at least one chip and on the other hand requiring the recited means for electrically connecting.

Therefore, it is irrelevant for the assessment of

clarity, whether the expression "comprises bonding wires" allows that further electrically conductive structures may participate in the desired interconnection, or whether the bonding wires should directly interconnect the respective pads. Moreover, it is irrelevant whether the skilled person could have difficulties in finding which other structures or arrangements would fall under the wording of the claim.

Consequently, claim 1 of the main request is clear in the sense of Article 84 EPC.

Inventive step

The device known from document D1 does not comprise the features of the second part of claim 1. In particular, in the known device, there is no electrical connection going from a second level interconnect **above** a first level interconnect through holes in the insulating layers of the first level interconnect, to chip bonding pads of said first interconnect. Moreover, in the specific form shown in Figure 6 of document D1, the electroconductive tracks do not extend between opposed rows of outer leads on respective opposed ends of the printed circuit. In particular, the outer leads of the first interconnect comprise pins or studs extending externally of the package.

The problem of high density packaging for modern chips having many bonding pads, particularly when a plurality of chips is packaged in a single package, i.e. the problem underlying the present invention, is not addressed in document D1.

Document D5 (see Figure 4 and the corresponding text)

concerns a semiconductor device comprising at least one semiconductor chip (34), the semiconductor chip (34) having a plurality of chip bonding pads (52), a package (42) which encloses the at least one semiconductor chip (34), a first level interconnect, which is a lead frame, with conductors (38) which extend externally of the package; the first layer interconnect is not covered by an insulating layer, and there is no incitation to provide such a supplementary insulating layer and to make first holes (through both insulating layers) to the chip bonding pads and second holes to pads of said "lead frame". There is in this document no disclosure of a printed circuit or of a multilayer insulating structure of the type disclosed in document D1.

Therefore, there would be no motivation to combine the teachings of these prior art documents and, in any case, such a combination does not lead to the semiconductor device of claim 1, which thus involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 Admissibility of the amendments

As indicated by the appellant, the amendments that the second level interconnect is located above the first level interconnect, that the plurality of bonding wires (38) each of which extends over the said one layer of

insulating material (26), and that, for the alternative, the array of electroconductive leads (100) each of which extends over the said one layer of insulating material (26), are based on the disclosure of the application as filed (see in particular page 7, lines 16 to 18, page 7, lines 32 to 36 and page 9, last line to page 10, line 4, respectively).

Therefore, the Board is satisfied that the European patent application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed (Article 123(2) EPC).

2.2 Clarity

2.2.1 Claim 1 as amended specifies that the second level interconnect is located above the first level interconnect comprising a printed circuit (8).

Moreover, according to the claim, for the first alternative, each of the bonding wires (38) of the plurality of bonding wires (38) of the second level interconnect extends over the one layer of insulating material (26) remote from the or each semiconductor chip.

Taking into account these added features for the first alternative, there is no ambiguity about the mutual arrangement of the chip bonding pads (36), the printed circuit (8) with the electroconductive tracks (20) and the bonding wires (38). In particular, the printed circuit (8) which overlies the chip (4) can be such that an interconnection by a bonding wire (38) can be formed between a chip bonding pad (36) on the chip and

a bonding pad (30) on an electroconductive track (20), the latter pad being accessible for the bonding wire (38) running over both the chip (4) and the insulating layer of the printed circuit. Thus, there is no contradiction in the claim between on the one hand requiring the printed circuit to overlie the at least one chip and on the other hand requiring the recited means for electrically connecting. Indeed, such an arrangement is shown in present Figures 1 to 5, in particular Figure 3.

In this respect, it is to be noted that the claim specifies for this first alternative that the means for electrically connecting of the second level interconnect "comprises" a plurality of bonding wires (38) each of which connects a respective bonding pad (30) to a respective chip bonding pad (36). However, since the meaning of these technical features is clear and since there is at least one way of carrying out the invention as claimed which is adequately disclosed in the application, the Board agrees with the appellant's submission that it is irrelevant for the assessment of clarity of the claim that the expression "comprises binding wires" allows that means other than the bonding wires may also participate in providing the interconnection.

It is also to be noted that, since in the present case the embodiment of the invention as described is consistent with the wording of the claim, the latter is adequately supported by the description as required by Article 84 EPC.

2.2.2 Furthermore, claim 1 specifies as a second alternative that the electroconductive leads (100) of the second

level interconnect extend over the layer of insulating material (94) remote from the semiconductor chip.

Therefore, it is considered that, for this second alternative, there is no ambiguity about the mutual arrangement of the chip bonding pads (98), the printed circuit with the electroconductive tracks and the electroconductive leads (100). In particular, the printed circuit (8) which overlies the upper surface (90) of the chip can be such that an interconnection by an electroconductive lead (100) can be formed between a chip bonding pad (98) on the chip and a respective via (96) on an electroconductive track (100), the via (96) being accessible for the electroconductive lead (100) running over both the chip and said insulating layer. Indeed, such an arrangement is shown in present Figures 6 to 8, in particular Figure 8.

2.2.3 Consequently, the Board is satisfied that claim 1 of the main request is clear in the sense of Article 84 EPC.

2.3 Novelty

The subject-matter of claim 1 does not form part of the state of the art and is thus new in the sense of Article 54 EPC.

2.4 Inventive step

2.4.1 Document D1 (see in particular the examples illustrated by Figures 5 and 6) discloses a semiconductor device which comprises a semiconductor chip (76; 94) having a plurality of chip bonding pads (96, 98), a package (72, 88; 92) which encloses the semiconductor chip (76; 94),

a first level interconnect (108) which extends externally of the package to provide a plurality of outer leads (74), and a second level interconnect comprising means (106, 114) for electrically connecting the chip bonding pads (96, 98) to selected contacts on the first level interconnect, which contacts overlie the at least one semiconductor chip (94). Moreover, there are insulating layers (99, 100, 102) separating the different layers of conductive means.

As submitted by the appellant, however, the device of document D1 does not comprise the features of the second part of claim 1. In particular, in this device, there is no electrical connection going from a second level interconnect **above** a first level interconnect through holes in the insulating layers of the first level interconnect, to bonding pads of said first interconnect. Moreover, in the specific form shown in Figure 6 of document D1, the electroconductive tracks do not extend between opposed rows of outer leads on respective opposed ends of the printed circuit. In particular, the outer leads of the first interconnect comprise pins or studs extending externally of the package.

The problem of high density packaging for modern chips having many bonding pads, particularly when a plurality of chips is packaged in a single package, i.e. the problem underlying the present invention, is not addressed in document D1.

Document D5 (see Figure 4 and the corresponding text) concerns a semiconductor device comprising a semiconductor chip (34) having a plurality of chip bonding pads (52), a package (42) which encloses the

semiconductor chip (34), a first level interconnect, which is a lead frame, with conductors (38) which extend externally of the package; the first layer interconnect is not covered by an insulating layer, and there is no incitation to provide such a supplementary insulating layer and to make first holes (through both insulating layers) to the chip bonding pads and second holes to pads of said "lead frame". There is in this document no disclosure of a printed circuit or of a multilayer insulating structure of the type disclosed in document D1.

Therefore, there would be no motivation to combine the teachings of these prior art documents and, in any case, such a combination does not lead to the semiconductor device of claim 1.

The other prior art documents are less relevant.

2.4.2 Therefore, having regard to the state of the art, the subject-matter of claim 1 was not obvious to a person skilled in the art. Thus, it involves an inventive step in the sense of Article 56 EPC.

2.5 Consequently, claim 1 is patentable in the sense of Article 52(1) EPC.

Therefore, a patent can be granted on the basis of claim 1 of the main request (Article 97(2) EPC).

3. Consequently, it is not necessary to consider the appellant's auxiliary requests.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of the following patent application documents:

Description:
Pages 2, 6 to 9, 13 and 14 as filed;
Pages 5, 10 to 12, 15 and 16 as filed with letter of 30 September 1993;
Page 4 as filed with letter of 26 July 1995;
Pages 1 and 3 as filed with letter of 11 May 2001;

Claims:
Nos. 1 to 6 as filed with letter dated 13 May 1997 (main request);

Drawings:
Sheets 1/5 to 5/5 as filed with letter of 30 September 1993.

The Registrar: The Chairman:

L. Martinuzzi R. K. Shukla