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D E C I S I O N
of 10 February 1999

Case Number: T 0578/97 - 3.5.1

Application Number: 91119207.8

Publication Number: 0492106

IPC: G01C 22/02

Language of the proceedings: EN

Title of invention:
Endurance management for solid state files

Patentee:
International Business Machines Corporation

Opponent:
Sandisk Corporation

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"
"Opposition - scope"

Decisions cited:
G 0009/91

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0578/97 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 10 February 1999

Appellant: (Opponent)
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Decision under appeal: **Decision of the Opposition Division of the European Patent Office posted 21 March 1997 rejecting the opposition filed against European patent No. 0 492 106 pursuant to Article 102(2) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: R. S. Wibergh
V. Di Cerbo

Summary of Facts and Submissions

I. The respondent is proprietor of European Patent No. 0 492 106, which is based on patent application No. 91 119 207.8 claiming priority of 28 December 1990.

II. The appellant (opponent) has opposed the patent in part, restricting the opposition to the subject-matter of claims 8 to 10. The ground for the opposition was that the subject-matter of these claims was either not new or did not involve an inventive step having regard in particular to the documents

D2: EP-A-0 392 895 and

D3: EP-A-0 349 775.

III. Claim 8 as granted reads as follows (omitting the reference signs):

A method for counting a number of erase/write cycles of a nonvolatile memory system including a plurality of nonvolatile memory blocks, at least one of said plurality of nonvolatile memory block containing no data and not having been previously accessed, the method comprising:

- counting a number of erase/write cycles that the plurality of nonvolatile memory blocks experience, respectively; and

- reallocating data contained in a first memory block to said at least one memory block when the counted number of erase/write cycles of said first

memory block is equal to a predetermined value.

IV. With decision dated 21 March 1997 the Opposition Division rejected the opposition.

V. The opponent lodged an appeal against this decision. In the statement setting out the grounds of appeal the view was maintained that D3 anticipated or at least rendered obvious the subject-matter of claim 8.

VI. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal, the Rapporteur expressed the preliminary opinion that the invention according to claim 8 had to be interpreted since the purpose of the last feature of the claim was not clearly derivable from the patent. Furthermore, it was doubted that the invention involved an inventive step over D3 when the general knowledge of a skilled person was taken into account. It was in particular noted that the possibility of replacing, during an erase/write cycle, either all or part of the data stored in a flash erase memory without loss of information was already known from D2.

VII. Oral proceedings were held on 10 February 1999.

VIII. The arguments brought forward by the parties can be summarised as follows:

The appellant:

In D3 it was stated that a block of an EEPROM (electrically erasable programmable read-only memory) which cannot be written any more must be replaced by a

new block. How this was to be done would depend on the circumstances. In case all the data in the old block had to be preserved, these data should be taken over by the new block. In case the old data were not needed any more, new data could be written into the new block during a normal erase/write cycle. Both options were obvious. Even the novelty of the method of claim 8 was questionable.

The respondent:

D3 did not render the invention obvious. When it was said in D3 that a block was "replaced" it merely meant that when the next time data were written, it would be to a new block. What happened to the data in the old block was not disclosed. D3 therefore did not teach to reallocate the data in the old block to the new block immediately upon having detected that the maximum allowable number of erasures had been reached, in accordance with the invention. It was even possible that the memory system in D3 had to cope with two addresses, one to the block of old data and one to the new block to be written.

The problem to be solved by the invention was to ensure that no data were lost when the old block could not be written any more. This might happen if the block was re-written only in part. D3 concerned flash memories, which are erased and written block-wise. Therefore the problem solved by the invention was not at all addressed in D3.

IX. The appellant requested that the decision under appeal be set aside and that the patent be revoked in respect

of claims 8 to 10.

X. The respondent requested that the appeal be dismissed and that the patent be maintained as granted (main request), or in amended form on the basis of claims 1 to 7 and 11 to 14 and a description to be amended (auxiliary request).

Reasons for the Decision

1. The appeal is admissible.

The respondent's main request

2. *The invention as claimed*

2.1 Claim 8 is directed to "a method for counting a number of erase/write cycles of a nonvolatile memory system", such as an EEPROM. The memory system comprises a plurality of nonvolatile blocks including blocks which have not been previously accessed. It is well known that EEPROM cells cannot be erased and written more than a certain number of times before the storage process becomes unreliable. To avoid that this happens, the number of erase/write cycles that the memory blocks experience are counted, and when the count is equal to a predetermined value the data contained in a block are "reallocated" to an unused block.

2.2 The meaning of the final "reallocating" feature of claim 8 has been discussed throughout the opposition proceedings. It is stated in the claim that the data

which are reallocated are "contained in a first memory block". This wording would normally imply that the data in question are actually *present* in the memory block, and are not simply associated with it in some way. The precision is necessary since, according to the description, the reallocation takes place during an erase/write cycle, and a write cycle implies that new data which may in general be entirely unrelated to the data contained at present in the memory block are to be stored in the memory. As the Board understands the claim, therefore, the reallocation process involves only data which have been taken from the first memory block. This also corresponds to the interpretation of the claim made in the appealed decision.

3. *Prior art*

D3 describes the closest prior art, which comprises - among other things - a method for counting a number of erase cycles of a nonvolatile memory. It mentions explicitly "flash" EEPROMs, which expression signifies memories in which entire groups of cells (such as a block) are erased at one go. The number of erase cycles experienced by each block is recorded and incremented by one for each cycle. This stored number is read out at the beginning of an erase/write cycle. Once it reaches a predetermined limit, the "block can be replaced automatically with a new redundant block" (column 11).

4. *Novelty*

The Board agrees with the Opposition Division that any difference between the invention and D3 can only lie in

the "reallocation" feature. The invention requires that data contained in a memory block which has reached the maximum number of erase/write cycles are reallocated, whereas according to D3 "a block can be replaced automatically with a new redundant block" when the critical limit has been attained. It is thus not explicitly said in D3 from where the data are taken which are written into the new block. The new data might originate from the old block, but they might just as well represent an arbitrary and complete replacement of the old data. Because of this ambiguity, the subject-matter of claim 8 is regarded as new.

5. *The technical problem to be solved by the invention*

5.1 The Board finds that it is useful to distinguish between two cases, neither of which is explicitly mentioned in the patent-in-suit. The first case is when the nonvolatile memory is updated block-wise, ie when completely new data are available for a whole block. The second case is when only a part of a block is updated and the rest of the data should remain unchanged.

5.2 In the first case it is difficult to see what purpose the invention might serve. If, during an erase/write sequence, a block must be reallocated, it appears pointless first to transfer the data from this block to a new one when a complete block of new data will anyway be written into the new block immediately afterwards. The only result, apparently, would be that the new block undergoes an unnecessary erase/write cycle. It is unlikely that a skilled person would understand the patent in this way.

5.3 If instead the second case is considered, the feature appears more meaningful: if the erase/write cycle involves only a partial update of the old block *the rest of the data* would be lost unless they are reallocated to the new block. The respondent has agreed that this is most probably the situation for which the invention is intended.

5.4 Compared with D3, the invention therefore solves the problem of saving any data which are contained in the old block and would be lost when, in connection with an erase/write cycle, the old block is replaced by a new one.

Since the skilled person generally cannot allow any data to be lost, this formulation of the problem does not contribute to an inventive step.

6. *Inventive step*

6.1 The respondent has argued that the claimed solution to the above problem cannot be rendered obvious by D3 alone or in combination with other documents since this prior art concerns a flash EEPROM in which blocks are erased and written block-wise. This was also the view of the Opposition Division.

6.2 The Board, however, cannot accept this reasoning.

D3 teaches that an old block, ie one which cannot safely be written any more, should be "replaced" by a new redundant block. In the Board's view this can only mean that all the data in the block should be transferred, in some suitable (but unspecified) way, to

the new block.

The respondent has suggested that according to D3 the old block would be retained and the system would subsequently have to keep track of two addresses, one to the old block and one to the new one. The old block would contain the data which have not been updated and the new block would contain the updates. This argument seems to have been accepted by the Opposition Division. The Board, however, finds that such an interpretation is contrary to the actual teaching of D3: if the old block is retained it has in fact *not* been replaced. Thus D3 does not suggest this possibility but, if anything, excludes it.

The Board instead understands D3 in the following way. If a complete set of new data are available the block replacement may certainly be performed in the form of a normal write cycle, as the Opposition Division noted. If however only a part of the block is to be updated during the write cycle - which is the more relevant situation, as noted at point 5.3 above - the rest of the data clearly have to be transferred (copied) from the old to the new block. In the Board's view, this follows directly from the teaching in D3 that the block should be replaced together with the requirement that no data may be lost. The consequence is that the method of claim 8 has to be regarded as obvious.

6.3 The Opposition Division seems to have been of the opinion that the invention involved an inventive step also because D3 (like the patent-in-suit) does not mention the possibility of a partial update of block data.

In fact there is nothing extraordinary about updating a block only in part. In D2, for example, it is noted in connection with "conventional" flash EEPROMs that "if not all the information in the chip is to be erased, the information must first be temporarily saved, and is usually written into another memory (typically RAM)" (column 5, lines 50 to 55).

D2 therefore proves - if proof is required - that the skilled person was aware that data are frequently updated only in part. It is therefore with this knowledge in mind that he would have tried to solve the technical problem, as outlined above.

6.4 In addition to the above argument, which is in principle based on D3 alone, the following argument based on a combination of D3 and D2 is also possible.

The quotation from D2 above shows not only that partial updates are well known but also that this technique normally requires that during an erase/write cycle data be transferred (from the EEPROM to RAM and back again) in order to avoid loss of information. This is an explicit hint to the solution of the current technical problem, as can be seen in the following way. D3 concerns the situation that data are to be written to a memory block when this block is found to have experienced the maximum number of erase/write cycles and therefore has to be "replaced". According to D2 block data which are not updated during a (normal) erase/write cycle should be read out, temporarily saved and written to the target block (which in this case is the block from which the data were read out). D3 together with D2 thus suggest a method of "replacing"

an old block by reading out the data contained in it, temporarily saving them and then writing them to the target block (which in this case is the new block). But this is already the "reallocation" feature of claim 8 as interpreted at point 2.2 above (since neither the claim nor any other part of the patent excludes that the reallocation is *via* a RAM).

The Board is unable to see what might possibly be inventive in such a combination. In particular, the respondent's argument that a system based on D3 would have to keep track of several block addresses simultaneously does not apply to this combination either. Only during the actual process of replacing the old EEPROM block by the new one would such a system have to manage more than one address. This is an isolated event. Afterwards, the single address to the new block suffices. The way blocks are addressed during the reallocation is not at all dealt with in the contested patent and could not serve to distinguish the invention from the prior art.

6.5 The Board thus concludes that the subject-matter of claim 8 does not involve an inventive step.

7. It follows that the appellant's request for revocation of the patent in respect of claim 8 is granted and the respondent's request for rejection of the appeal is refused.

The respondent's auxiliary request

8. The respondent's auxiliary request is that the patent be maintained on the basis of the claims which have not

been opposed. Since this part of the patent is not subject to an opposition the Board has no power either to examine it or to decide on it (cf G 9/91, OJ 1993, 408). This request is therefore granted.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to maintain the patent in amended form on the basis of claims 1 to 7 and 11 to 14 and a description to be amended.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg