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DECISION of 4 April 2001

Case Number: T 0570/97 - 3.4.3

Application Number: 90307351.8

Publication Number: 0408252

IPC: H01L 29/73

Language of the proceedings: EN

Title of invention:

Heterojunction bipolar transistor

Applicant: AT&T Corp.

Opponent:

Headword:

Bipolar transistor/AT&T

Relevant legal provisions:

EPC Art. 111(1)

Keyword:

"Remittal (yes) - claims substantially amended"

Decisions cited:

T 1032/92

Catchword:



Europäisches Patentamt

European **Patent Office**  Office européen des brevets

Beschwerdekammem

Boards of Appeal

Chambres de recours

Case Number: T 0570/97 - 3.4.3

DECISION of the Technical Board of Appeal 3.4.3 of 4 April 2001

Appellant:

AT&T Corp.

32 Avenue of the Americas New York, NY 10013-2412 (US)

Representative:

Watts, Christopher Malcom Kelway, Dr.

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Decision under appeal:

Decision of the Examining Division of the

European Patent Office posted 13 March 1997 refusing European patent application

No. 90 307 351.8 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman:

R. K. Shukla

Members:

G. L. Eliasson

A. C. G. Lindqvist

## Summary of Facts and Submissions

I. European patent application No. 90 307 351.8 was refused in a decision of the examining division dated 13 March 1997. The ground for the refusal was that the subject matter of claim 1 as amended according to the request dated 7 March 1996 and the subject matter of claim 7 as amended according to the applicant's requests dated 7 March 1996 and 12 July 1994 did not involve an inventive step having regard to the prior art documents

D1: IEEE Electron Device Letters, vol. 10, no. 5, May 1989, pages 200 to 202; and

D2: IEEE Transactions on Electron Devices, vol. ED-34, no. 2, February 1987, pages 185 to 197.

- II. The independent claims 1 and 7 as refused by the examining division read as follows:
  - "1. An Article comprising a heterojunction bipolar transistor comprising a semiconductor body comprising an emitter region, a collector region, and a base region (14) between the emitter and the collector regions, and further comprising means for making electrical contact with the emitter, base, and collector regions, respectively, with the emitter region comprising first semiconductor material that has a larger bandgap than the base region material and is of the opposite conductivity type from the base region material, the emitter region and base region being epitaxial with each other and with the collector region, associated with the transistor are bias

voltages within a normal operating range of the transistor, associated with the emitter region being an emitter stripe width W, associated with the base region being an "extrinsic" base region;
CHARACTERIZED IN THAT

- (a) the emitter region comprises a layer (15) of first semiconductor material that overlies essentially all of the base region, the thickness of the layer chosen such that the portion of the layer that overlies the extrinsic base region is substantially fully depleted of conduction electrons at all bias voltages within the normal operating range of the transistor; and
- (b) the means for making electrical contact to the base region comprise a region on the layer of first semiconductor material that provides an ohmic contact with the base region."
- "7. A method of producing an Article comprising a heterojunction bipolar transistor as claimed in any of the preceding claims; the method comprising
- (a) providing a semiconductor substrate with a multiplicity of semiconductor layers thereon, the multiplicity comprising, in sequence, a collector layer of a first conductivity type, a base layer of a second conductivity type, an emitter layer of the first conductivity type, and at least one further layer on the emitter layer, the material of the emitter layer chosen to have a larger bandgap than the material of the base layer;
- (b) removing the at least one further layer in selected regions, thereby exposing selected portions of the emitter layer in the semiconductor body; and

- (c) providing the means for making electrical contact with the emitter, base and collector regions; CHARACTERIZED IN THAT the method further comprises
- (d) removing selected portions of the emitter layer and of the base layer such that the emitter layer covers essentially all of the base layer in the semiconductor body; and
- (e) step (c) comprises causing the formation of an ohmic contact between a region on the emitter layer and the base region."
- III. The appellant (applicant) lodged an appeal together with a statement of the grounds of appeal on 6 May 1997 and paid the appeal fee the same day. New claims 1 to 5 were filed with the statement of the grounds of appeal.

The appellant requests that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 5 filed with the statement of the

grounds of appeal

Description: pages 1 to 9 as filed, and incorporating

amendments as requested in the statement

of the grounds of appeal

Drawings: Sheets 1/4 to 4/4 as filed.

- IV. Claim 1 in accordance with the appellant's request reads as follows:
  - "1. A method of making a bipolar transistor comprising
  - (a) providing a semiconductor substrate (11) with a multiplicity of semiconductor layers thereon, the multiplicity comprising, in sequence, a collector layer (13) of a first conductivity type, a base layer (14) of a second conductivity type, an emitter layer (15) of the first conductivity type, and at least an emitter contact layer (19) of the first conductivity type; and
  - (b) providing means for making electrical contact with the emitter layer, base layer and collector layer, respectively;

CHARACTERIZED IN THAT the method further comprises

- (c) patterning the emitter contact layer and any further semiconductor layer disposed thereon such that an emitter stripe (19) of width W < 1  $\mu$ m remains and a predetermined region of the emitter layer is exposed; and in that step (b) comprises
  - (i) simultaneously depositing, in self-aligned fashion, emitter contact metal (23) and base contact metal (16), the base contact metal disposed on the emitter layer (15) and spaced from the emitter stripe (19), the emitter contact metal (23) disposed on the emitter stripe or any further semiconductor material disposed thereon; and
  - (ii) heat treating the substrate with the multiplicity of semiconductor layers thereon such that base contact metal diffuses

through the emitter layer (15) and into the base layer (14), substantially without diffusion of base contact metal into the collector layer."

Claims 2 to 5 are dependent on claim 1.

V. The appellant argued essentially that the simultaneous and self-aligned deposition of the emitter and base contact metal, with the base contact metal spaced from the emitter stripe by a small amount, as specified in claim 1, is not disclosed or suggested by the cited references.

## Reasons for the Decision

- 1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.
- The amended set of claims according to the appellant's request contains only one independent method claim 1 corresponding to the method claim 7 forming the basis of the decision under appeal, there being no independent claim corresponding to the device claim 1 which was refused in the decision under appeal.

With respect to the independent method claim 7 which was considered to be contravening the requirement of inventive step in the decision under appeal, the subject matter of claim 1 presently under consideration

(A) has been broadened to cover a method of producing a bipolar transistor, in contrast to the former method claim which was restricted to a method of producing a heterojunction bipolar transistor having the bandgap of the emitter layer larger than that of the base layer; and specifies that the

- (B) width W of the emitter stripe (19) is less than 1  $\mu$ m (step c));
- (C) the emitter and base contact metals are deposited simultaneously and in a self-aligned fashion (step (b)(i)); and
- (D) the substrate is heat treated to diffuse base contact metal through the emitter layer (step (b)(ii)).

Neither features (A), (C) nor (D) were previously claimed. Although feature (B) is present in claim 2 as filed, it was claimed together with the requirement that the thickness of the emitter stripe is in the range of 5 to 24 nm.

3. The above amendments to claim 1 which the appellant has submitted in the appeal proceedings raise a number of new issues which were not considered during the examination proceedings. Firstly, it needs to be considered whether the amendments comply with the requirements of Article 123(2) EPC. Secondly, the arguments given in the statement of the grounds of appeal regarding inventive step concentrate on the steps of forming the emitter and base contact metals (features (C) and (D)). These process steps were however not claimed previously and were therefore not considered in the assessment of inventive step during the examination proceedings.

4. In the present case, since the appellant no longer seeks grant of a patent including the subject matter as rejected by the examining division, but has filed a substantially amended text for claim 1 which requires substantial further examination in relation to both the formal and substantive requirements of the Convention, it is clearly appropriate that the case should be remitted to the examining division in accordance with Article 111(1) EPC.

The Board also refers to Decision T 1032/92 (not published in the OJ EPO), where it was stated that the filing of a new request for the first time in the statement of the grounds of appeal, as in the present case, inevitably leads to undesirable procedural delay.

## Order

## For these reasons it is decided that:

- 1. the decision under appeal is set aside.
- The case is remitted to the department of the first instance for further examination of the application having regard to the request as set out in the statement of the grounds of appeal.

The Registrar:

The Chairman:

L. Martinuzzi

R. K. Shukla

