

**Internal distribution code:**

- (A) [ ] Publication in OJ  
(B) [ ] To Chairmen and Members  
(C) [X] To Chairmen  
(D) [ ] No distribution

**D E C I S I O N**  
of 9 July 2001

**Case Number:** T 0455/97 - 3.4.3

**Application Number:** 91200496.7

**Publication Number:** 0451883

**IPC:** H01L 27/112

**Language of the proceedings:** EN

**Title of invention:**

Process for the accomplishment of an ROM memory cell having a low drain capacity

**Applicant:**

STMicroelectronics S.r.l.

**Opponent:**

-

**Headword:**

-

**Relevant legal provisions:**

EPC Art. 123(2), 56

**Keyword:**

"Additional subject-matter (no - after further amendments)"  
"Inventive step (yes), not an obvious combination of the prior art documents having regard to the problem"

**Decisions cited:**

-

**Catchword:**

-



Europäisches  
Patentamt

European  
Patent Office

Office européen  
des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Case Number: T 0455/97 - 3.4.3

**D E C I S I O N**  
of the Technical Board of Appeal 3.4.3  
of 9 July 2001

**Appellant:** STMicroelectronics S.r.l.  
Via C. Olivetti, 2  
20041 Agrate Brianza (Milano) (IT)

**Representative:** Mittler, Enrico  
c/o Mittler & C. S.r.l.  
Viale Lombardia, 20  
20131 Milano (IT)

**Decision under appeal:** Decision of the Examining Division of the European Patent Office posted 9 December 1996 refusing European application No. 91 200 496.7 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** M. Chomentowski  
M. B. Günzel

## Summary of Facts and Submissions

I. The appellant is the applicant for the European patent application No. 91 200 496.7 (Publication No. 0 451 883), which was filed with 3 claims reading as follows:

"1. Process for the accomplishment of an ROM memory cell having a low drain capacity, comprising the formation of a gate complex (10) on a part of a substrate (1) of semiconductor material which shall form the cell's channel region and a subsequent step of n- implantation outside said channel region for the formation of regions of source (5) and drain (6) having n- doping, characterized in that it subsequently comprises the masking of the drain region (6) and of an adjacent part of the gate complex (10) and a subsequent step of n+ implantation for the creation of an area (9) having n+ doping in said source region (5)."

"2. Process according to claim 1, characterized in that it includes the formation of spacers (7) to the sides of said gate complex (10) after said n- implantation and before said masking."

"3. ROM memory cell obtained with the above process, comprising a substrate (1) of semiconductor material, a gate complex (10) superimposed over a channel region of said substrate (1) and regions of source (5) and drain (6) obtained in said substrate (1) to the sides of said gate complex (10), characterized in that at least one part of said drain region (6) has low doping with respect to said source region (5)."

II. The application was refused by the examining division by a decision of 9 December 1996 on the ground that the application as amended did not comply with the requirement of Article 123(2) EPC since it contained subject-matter which extended beyond the content of the application as filed.

Moreover, according to the decision under appeal, claims 1 and 3 lacked an inventive step having regard to the prior art documents

D1: Patent Abstracts of Japan, vol. 13, no. 304  
(E-786) [3652] 12 July 1989; & JP-A-1 081 360; and

D2: EP-A-0 227 965.

III. In the decision under appeal, the examining division reasoned essentially as follows:

**Admissibility of the amendments**

Claim 1 of the text forming the basis for the decision contained the amendment "protecting ... a channel-side part of the source region (5)". Thus, the originally disclosed step of providing a gate sidewall spacer, which is a specific form of "protecting" implying self-alignment and a relatively small lateral dimension, had been unjustifiably generalised in one of "protecting" the channel-side part of source region. Indeed, a step of protecting (or masking) is a broad term which covers applying a photoresist or mask, aligning and patterning, and a skilled person would not directly derive "gate spacers" from the term "protecting means".

Therefore, the application contained additional subject-matter.

**Inventive step**

Document D1 discloses a process for making a ROM cell whereby a resist mask is formed on the entire drain region and an adjacent part of the gate complex for obtaining an entirely n+ doped source region (47) and an entirely n- doped drain region (45). On the contrary, in particular in the process comprising the features of claim 1 and claim 2, a channel-side part of source region is also protected, this leading to a n-doped portion of the source region adjacent the channel and hence to a lower electric field.

The problem to be solved by the present invention may therefore be regarded as the reduction of hot electron effects caused by high electric fields.

Document D2 solves this particular problem by the method step of protecting or masking the channel-side part of the source region from being heavily doped.

The skilled person would therefore regard it as a normal design option to include this feature in the process described in document D1 in order to solve the problem posed, so that the claimed process lacked an inventive step.

The same reasoning applies with equal strength to the device of claim 3. This device has a channel-side part of the source region which is n- doped and differs only in that sense from the device known from document D1. However, this feature has already been employed for the same purpose of reducing high electric fields at the source to channel junctions in the similar device known from document D2.

Therefore, the claimed device also lacked an inventive step.

- IV. The applicant lodged an appeal against this decision on 6 February 1997 paying the appeal fee on 15 February 1997.

With the statement setting out the grounds of appeal, which was filed on 7 April 1997, the appellant maintained as his main request the set of 3 claims forming the basis for the decision under appeal and filed an auxiliary request consisting of a method claim based on a combination of claims 1 and 2 of the main request, and an independent device claim 2 corresponding to claim 3 of the main request.

Moreover, the appellant requested oral proceedings auxiliarily.

- V. With a communication dated 16 March 2001, the Board informed the appellant that the independent claims 1 and 3 of the main request and the independent claims 1 and 2 of the auxiliary request appeared to contain subject-matter which extended beyond the content of the application as filed, but that new claims 1 and 2 based on the auxiliary request and containing further minor amendments could be allowable.

- VI. With letter dated 9 May 2001 the appellant expressed his agreement to the proposed claim and filed new claims 1 and 2 with an adapted page 3 of the description.

Claims 1 and 2 read as follows:

"1. Process for manufacturing a ROM memory cell having a low drain capacity, comprising the following steps:

- (a) formation of a gate complex (10) on a part of a substrate (1) of semiconductor material which shall constitute the cell's channel region;

- (b) n- implantation outside said channel region to form n- doped source (5) and drain (6) regions;
- (c) formation of spacers (7) to the sides of said gate complex (10) so that one of them covers a channel-side part of the source (5) region;
- (d) masking of the entire drain region (6) and an adjacent part of the gate complex (10);
- (e) n+ implantation for creating an n+ doped remaining part (9) of said source region (5)."

"2. ROM memory cell comprising a substrate (1) of semiconductor material, a gate complex (10) superimposed over a channel region of said substrate (1), and ion implanted source (5) and drain (6) regions obtained in said substrate (1) at the sides of said gate complex (10), characterized in that said drain region (6) and a channel-side part of the source region (5) are n- doped and the remaining part (9) of the source region (5) is n+ doped."

VII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following patent application documents:

**Description:** Pages 1, 2, 4 and 5, filed with applicant's letter dated 20 December 1993;  
Page 3 filed with appellant's letter dated 9 May 2001;

**Claims:** Nos. 1 and 2 filed with appellant's letter dated 9 May 2001; and

**Drawings:** Sheet 1 as originally filed.

The appellant submitted the following arguments in support of his request:

**Admissibility of the amendments**

A person skilled in the art understands from page 4 of the application as filed that a part of the source region, the entire drain region and a part of the gate complex are to be covered by the protecting means, whereby a gate spacer, disclosed in claim 2 as filed, is appropriate for covering a source part of small lateral dimension. Present claim 1 is restricted to such a process, so that the application contains no additional subject-matter.

**Inventive step**

The present invention concerns ROM memory cells having a low drain capacity. As can be seen from the introduction of the present application, the problem of reducing the drain capacitance is typical of memory cells arranged in NOR type arrays, that is connected in parallel and with all drains connected together.

On the contrary, document D1 discloses MISFET devices arranged in a different kind of array, that is, serially connected with the source region of a MISFET directly connected with the drain region of the adjacent MISFET. This can be understood from Figure 5 of document D1, i.e., the last Figure of the abstract, wherein each region (47) is a part of the drain region of left-hand MISFET and the source region of the right-hand MISFET as well.

As mentioned in document D1, it is important in this kind of MISFET array to reduce the source-drain resistance in order to enhance the current driving capability of the entire assembly of serially connected



MISFETs. This object is obtained by forming the drain of each MISFET as a low concentration layer (45) at its channel side and as a high concentration layer (47) at the other section. The MISFETs of group B are made according to the abstract and solve this problem.

On the other hand, the structure of the MISFETs of group C is not described in the abstract and cannot be understood from the drawings, in particular Figures 5 and 6, in the corresponding Japanese patent application.

Therefore, document D1 does not teach process steps for causing the entire drain region to be doped at low concentration and, moreover, no mention is made, at least in the abstract, of an interest to obtain low drain capacitance, which is not a problem for the known devices in the arrangement shown in the document.

On the other hand, document D2 is concerned with a different technical problem, which is to reduce high electric fields at the sides of the channel region, and it does not comprise any indication about reduction of drain capacitance. Therefore, the document does not provide any useful teaching which can be combined with that of document D1 to solve the drain capacitance problem of the claimed invention. Therefore, the claimed invention involves an inventive step.

## Reasons for the Decision

1. The appeal is admissible
2. *Admissibility of the amendments*
  - 2.1 Present claim 1 concerns a process for manufacturing a ROM memory cell having a low drain capacity, comprising the following steps:
    - (a) formation of a gate complex (10) on a part of a substrate (1) of semiconductor material which shall constitute the cell's channel region;
    - (b) n- implantation outside said channel region to form n- doped source (5) and drain (6) regions;
    - (c) formation of spacers (7) to the sides of said gate complex (10) so that one of them covers a channel-side part of the source (5) region;
    - (d) masking of the entire drain region (6) and an adjacent part of the gate complex (10);
    - (e) n+ implantation for creating an n+ doped remaining part (9) of said source region (5).

- 2.1.1 Present claim 1 results essentially from the combination of claim 1 and dependent claim 2, both as filed, and thus comprises the formation of spacers (7) to the sides of the gate complex (10) before the step of n+ implantation.

The feature "protecting ... a channel-side part of the source region (5)" of claim 1, which was considered as an unallowable generalization under Article 123(2) EPC by the examining division, is thus replaced by the

wording "formation of spacers ... so that one of them covers a channel-side part of the source (5) region" in the present claim. Thus, the objection under Article 123(2) EPC raised in the decision under appeal has been overcome by these amendments.

The further feature of present claim 1 that, after the step of n- implantation for forming the source (5) and drain (6) region outside the gate complex (10) and before the step of n+ implantation, the process comprises masking or protecting the entire drain region (6), had not been objected by the examining division and has indeed a basis in the application as filed (see page 4, lines 16 to 18 and page 3, lines 13 to 21).

- 2.2 Present claim 2 concerns a ROM memory cell comprising a substrate (1) of semiconductor material, a gate complex (10) superimposed over a channel region of said substrate (1), and ion implanted source (5) and drain (6) regions obtained in said substrate (1) at the sides of said gate complex (10), characterized in that said drain region (6) and a channel-side part of the source region (5) are n- doped and the remaining part (9) of the source region (5) is n+ doped.

Present claim 2 is essentially identical with claim 3 of the application as filed whereby in particular the statement in the original claim that the device is "obtained by the above process" is replaced by specifying that the source and drain regions (5, 6) are ion implanted regions, this being the only doping method disclosed in the application as filed.

2.3 Further amendments to the application are mainly for adapting the description to the new claims. The Board is therefore satisfied that the application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed (Article 123(2) EPC).

3. *Inventive step*

3.1 The only other issue in the present appeal is that of inventive step of claims 1 and 2.

It has not been disputed that document D1, which consists of an abstract in English language of a Japanese patent application, represents the closest prior art.

A process for making an integrated circuit comprising insulated-gate field effect transistors (MISFETs) is known from document D1 (see, in the abstract, the "Constitution"); in a region "B" showing two memory cells, the process comprises the following steps:

- (a) formation of a gate complex (43, 44) on a part of a substrate (40) of semiconductor material which shall constitute the cell's channel region;
- (b) n- implantation outside said channel region to form n- doped source and drain regions (45);
- (d) masking of a part of the drain region (45) and an adjacent part of the gate complex (43, 44) with a resist film (46);
- (e) n+ implantation for creating an n+ doped part (47) of said source region (45).

3.1.1 However, contrary to the process of present claim 1, the known process does not comprise, after the n-implantation and before the masking,

(c) the formation of spacers (7) to the sides of said gate complex (10) so that one of them covers a channel-side part of the source (5) region.

Since in the known process there is no spacer to the sides of the gate complex and thus no corresponding masking of the part of said source region covered by the spacer on the source side, there is the further distinguishing feature that there is left no n- doped part of the source in a channel-side part of said source and thus no creation of an n+ doped "remaining" part (47) of said source region (45).

This is indeed in accordance with the "Purpose" in the abstract of document D1 (see the "Purpose"), to reduce a resistance between a source and a drain and to enhance a current driving capacity by forming the source only of a high concentration layer.

It is also to be noted that, according to the "Purpose" in document D1, it is intended to form the drain of a low concentration layer at the end of a channel side and of a high concentration layer at the other section. Thus, there is no step such as in present step d) of masking of the **entire** drain region (45) with a resist film (46).

3.2 Indeed, in the fabrication process known from document D2 (see Figures 4 and 5 and the corresponding text), there is a step of formation of spacers (20) to the sides of a gate complex (4, 3) so that one of them covers a channel-side part of the source region (16).

3.3 However, the appellant has convincingly argued as follows with respect to the documents D1 and D2:

The present invention concerns ROM memory cells having a low drain capacity.

Document D1 discloses MISFET devices arranged in an array wherein the source region of a MISFET is directly connected with the drain region of the adjacent MISFET. This can be seen in Figure 5 of document D1, i.e., the last Figure of the abstract, wherein each region (47) is a part of the drain region of left-hand MISFET and the source region of the right-hand MISFET as well.

As mentioned in document D1, it is important in this kind of MISFET array to reduce the source-drain resistance in order to enhance the current driving capability of the entire assembly of serially connected MISFETs. This object is obtained by forming the drain of each MISFET as a low concentration layer (45) at its channel side and as a high concentration layer (47) at the other section. The MISFETs of group B are made according to the abstract and solve this problem.

On the other hand, the structure of the MISFETs of group C is not described in the abstract and cannot be understood from the drawings, in particular Figures 5 and 6, in the corresponding Japanese patent application.

Therefore, document D1 does not teach process steps for causing the entire drain region to be doped at low concentration.

Moreover, document D1 does not mention the problem of high drain capacitance, and this problem is apparently not known to occur in the array of devices shown in the document.

With regard to document D2, it is concerned with a different technical problem, which is to reduce high electric fields at the sides of the channel region, and it does not comprise any indication about reduction of drain capacitance. Therefore, the document does not provide any useful teaching which can be combined with ~~that of document D1 to solve the drain capacitance~~ problem of the claimed invention.

In any case, there is no teaching in either of the documents D1 and D2 to form a memory cell wherein the entire drain region is at low concentration, in order to have a low drain capacitance.

- 3.4 For the foregoing reasons, in the Board's judgment, the subject-matter of present claim 1 is not obvious to a person skilled in the art and it thus involves an inventive step in the sense of Article 56 EPC. Consequently, present claim 1 is patentable in the sense of Article 52(1) EPC.
- 3.5 Claim 2 concerns a device having the same device features as those obtained by the process of claim 1. In particular, the entire drain region has the low doping concentration providing low drain capacitance. The above reasoning in respect of claim 1 therefore applies to claim 2, which accordingly involves an inventive step.
4. Consequently, oral proceedings, requested auxiliarily by the appellant, are not needed.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the examining division with the order to grant a patent on the basis of the following patent application documents:

**Description:** Pages 1, 2, 4 and 5, filed with letter dated 20 December 1993;  
Page 3 filed with letter dated 9 May 2001;

**Claims:** Nos. 1 and 2 filed with letter dated 9 May 2001; and

**Drawings:** Sheet 1 as originally filed.

The Registrar:

R. Schumacher

The Chairman:

R. K. Shukla

MCA