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D E C I S I O N
of 24 October 2001

Case Number: T 0428/97 - 3.4.3

Application Number: 90111438.9

Publication Number: 0404008

IPC: H01L 27/02

Language of the proceedings: EN

Title of invention:
Substrate bias generation circuit used in semiconductor integrated circuit

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0428/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 24 October 2001

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 2 December 1996 refusing European patent application No. 90 111 438.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
M. J. Vogel

Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division to refuse European patent application No. 90 111 438.9 dated 2 December 1996. The ground for the refusal was that the invention as claimed did not involve an inventive step (Article 56 EPC). The decision under appeal refers *inter alia* to the documents:

D1: EP-A-0 022 870, and

D2: EP-A-0 024 903.

II. The appellant (applicant) lodged an appeal which was received 31 January 1997. The appeal fee was payed the same day. The statement of the grounds of appeal was received 2 April 1997.

The appellant requested that the decision of the examining division be set aside and that a patent be granted on the basis of claims 1 to 4 filed with the letter of 24 September 2001.

III. The wording of the independent claim is as follows:

"1. A CMOS DRAM memory device comprising

a semiconductor substrate (10) having inner resistance and capacitance;

a MOS memory integrated circuit (12) including MOS transistors of enhancement type formed on said semiconductor substrate (10); and

substrate bias generation circuit means arranged on said semiconductor substrate (10), for absorbing carriers which are injected from said MOS memory integrated circuit (12) into said semiconductor substrate (10) through the inner resistance and the capacitance;

wherein

said substrate bias generation circuit means comprises a plurality of substrate bias voltage generation circuits including first and second substrate bias voltage generation circuits (11A, 11B);

said bias voltage generation circuits (11A, 11B) are respectively arranged at opposite sides of said MOS memory integrated circuit (12), to thereby minimize a temporal and local variation of a desired substrate potential, which is caused by carriers, wherein the arrangement of said bias voltage generation circuits (11A, 11B) satisfying the following conditions:

a time constant (T) of current flowing into said first and second substrate bias voltage generation circuits (11A, 11B) through the inner resistance (R/2) and the capacitance (C/2) of said semiconductor substrate (10) is at a minimum value (T0/4), and

a distance from said first substrate bias voltage generation circuit (11A) to a portion of said MOS memory integrated circuit (12) furthest from said substrate bias voltage generation circuit (11A) is substantially equal to a distance from said second substrate bias voltage generation circuit (11B) to a portion of said MOS memory integrated circuit (12)

furthest from said second substrate bias voltage generation circuit (11B); and

said first and second substrate bias voltage generation circuits (11A, 11B) are respectively allocated to equally divided areas of said MOS memory integrated circuit (12)."

IV. The appellant argued essentially as follows:

- Contrary to what is disclosed in the prior art documents, the claimed memory device comprises at least two substrate bias voltage generation circuits located on different positions of the semiconductor substrate in order to evenly absorb the surplus carriers in the substrate in consideration of its inner resistance and capacity. Although in the prior art the importance of reducing variations of the substrate bias potential has been recognized, this was not the case with respect to the necessity of restricting to a minimum the temporal and local variations of the substrate's potential. It is for the first time that transient processes and the time dependence of the substrate bias voltage has been taken into account.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments (Articles 84 and 123(2) EPC)*

The claims have been amended in the course of the appeal proceedings. Although, these amendments are not discussed in detail here, as the appeal did not succeed

for the reasons which follow, they comply wit the requirements of Articles 123(2) and 84 EPC.

3. *Inventive step (Article 56 EPC)*

3.1 Document D1 discloses a CMOS DRAM (Complementary Metal-Oxide-Semiconductor Dynamic Random Access Memory) memory circuit comprising a substrate bias generation circuit 17 which absorbs the so-called substrate current. This current is formed by carriers which are generated by impact ionization in the channel region of the transistors and are injected into the substrate. Since in a dynamic type memory circuit the operating frequency is variable, the bias generation circuit disclosed in this document is formed by a first generator that absorbs a magnitude of the substrate current proportional to the operating frequency and by a second generator whose output is independent of the operating frequency. However, as shown in Figure 1, both generators are placed on the same area of the substrate and form, in fact, a single generator (cf. page 1, lines 4 to 8; page 2, lines 13 to 17; page 3, lines 22 to 34).

3.2 The memory device according to claim 1 of the present application differs from this known memory device essentially in that

- at least two substrate bias voltage generation circuits (11A, 11B) are provided on opposite sides of the memory integrated circuit in order to minimize temporal and local variations of the desired substrate potential.

3.3 According to the application, it is an object of the

invention to prevent that in a relatively large, high-speed semiconductor memory the substrate potential deviates transiently and locally from a preset value due to the carriers injected into the substrate (cf. column 2, line 52 to column 3, line 6).

The provision of at least two substrate bias voltage generation circuits on different locations of the substrate reduces the resistance and capacity of the substrate area allocated to each bias circuit. Consequently, the time constant of the current flowing in the substrate is reduced with respect to the situation in which only a single bias circuit is present and a higher degree of temporal stability of the substrate's potential can be realized (cf. column 3, lines 23 to 31).

3.4 The Board concurs with the appellant in that documents D1 and D2 do not addresses explicitly the problem of temporal variations of the substrate's potential and that these documents are mainly concerned with improving the electric properties of a single biasing circuit. However, both documents underline the importance of maintaining the substrate bias voltage at a desired value to avoid malfunctions of the memory device.

Document D1 discloses that the level of the threshold voltage must be maintained at a desired optimum level. The memory device becomes either unstable and susceptible to noise or cannot be operated at high switching speeds if the threshold voltage is below or above this level, respectively. The substrate bias voltage generator assures that the threshold voltage is maintained at this preset level (cf. "Background art",

page 1, lines 10 to 29).

Also document D2 discloses that variations of the threshold voltage causes malfunctions of the memory device due to variations of the potentials of the input signals. A substrate bias voltage generator is, therefore, provided for maintaining the substrate potential at the desired value. In this document a substrate bias generating circuit is provided for generating a stable substrate potential and for reducing variations in the substrate potential due *inter alia* to variations of the substrate current (cf. page 1, lines 5 to 26 and page 2, lines 1 to 5 and 22 to 25).

The skilled person in the art was, therefore, aware that the substrate's potential had to be maintained at an optimum level. Furthermore, he would carefully consider the substrate biasing, as it is disclosed in documents D1 and D2 that a possible cause of malfunction of the memory device is the departure of the substrate bias voltage form this desired level.

3.5 The appellant has argued that it is the first time that the local variations and the transient behaviour of the substrate bias voltage has been taken into account.

The Board, however, cannot follow this argument, since the specification in documents D1 and D2 that the substrate potential should be maintained at the optimum level implies that any departure from this optimum level should be corrected as fast as possible, i.e. the bias circuit must quickly respond to any voltage variations due to the injected carriers to compensate effectively any temporal departures. The same is true

with respect to local variations of the substrate's potential, since according to these documents they would generate local malfunctions of the memory device.

In the Board's view, the skilled person would realize from the teaching of documents D1 and D2 that in order that the biasing circuit effectively removes the injected current and thereby avoids the malfunctions of the device, the time delay introduced by the substrate has to be taken into account.

3.6 In relatively small memory devices local and temporal stability of the substrate's potential can be assured by a single biasing circuit, since the time delay introduced by the substrate is relatively small.

However, the technological development of integrated circuit memory devices has lead to steadily increasing memory capacities which are operated at always higher frequencies. The temporal and local stability of the substrate bias voltage in these devices becomes more relevant due to the increased size of the semiconductor chip.

A skilled person would, therefore, also take into account the resistance and capacitance of the substrate when designing the substrate bias voltage circuit. These considerations would lead the skilled person to reduce the time constant associated with the transmission of signals in the substrate by reducing the area of the memory device biased by a single biasing circuit and, consequently, to provide a plurality of biasing circuits on the memory device. To allocate an equal area of the substrate to each one of these biasing circuits, as set out in claim 1 of the

application in suit, would be an alternative obvious to the skilled person.

3.7 For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 does not involve an inventive step in the sense of Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla