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D E C I S I O N
of 1 December 1998

Case Number: T 0200/97 - 3.5.1

Application Number: 87906599.3

Publication Number: 0285667

IPC: G05B 19/04

Language of the proceedings: EN

Title of invention:
Sequence controller

Patentee:
Hitachi, Ltd.

Opponent:
Siemens AG

Headword:
Sequence controller/HITACHI

Relevant legal provisions:
EPC Art. 52(1), 56, 114(2)

Keyword:
"Inventive step - yes"

Decisions cited:
T 0085/93

Catchword:
-

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Case Number: T 0200/97 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 1 December 1998

Appellant: (Opponent)
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Representative:
-

Respondent: (Proprietor of the patent)
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Decision under appeal:
Decision of the Opposition Division of the European Patent Office posted 13 December 1996 rejecting the opposition filed against European patent No. 0 285 667 pursuant to Article 102(2) EPC.

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: R. Randes
S. C. Perryman

Summary of Facts and Submissions

I. The opposition by the appellant to European patent No. 285 667 in the name of the respondent was rejected by the opposition division in the decision under appeal. As granted, claim 1 (subdivided for ease of reference into features F1 to F8 as in the appealed decision and the statement of grounds) reads:

"A sequence controller (1) comprising:

F1: a program storage means (22) for storing a sequence program; external signal input terminals divided into multiple blocks (3a), at least one block being subdivided into multiple groups (1a), each group consisting of multiple terminals (t1....tn);

F2: an arithmetic and logic operation means (21b) having a timing signal generating circuit for producing a timing signal, the arithmetic and logic operation means (21b) being adapted to perform logic operation on two or more signals including the external signals taken in from the external signal input terminals, according to a sequence program read out from the program storage means (22) in synchronism with the timing signal;

F3: an output means for outputting a control signal according to the result of operation performed by the arithmetic and logic operation means (21b); characterised in that

F4: first signal generating means (Ia1, Ia2) disposed

for each one of said groups for outputting a first signal when a signal calling for an interrupt processing comes to at least one of said multiple terminals (t1) associated with a particular group;

F5: second signal generating means (3a, 3b) disposed for each one of said blocks for outputting a second signal when at least one of said multiple groups associated with a particular block outputs the first signal;

F6: a second signal transfer means for informing the arithmetic and logic operation means (21b) that the second signal has occurred in one of the blocks; and

F7: an access means by which the arithmetic and logic operation means (21b) when informed by the second signal transfer means of the occurrence of the second signal stops the logic operation required by the sequence program, accesses the second signal generating means successively

F8: and, when it finds the particular second signal generating means that has produced the second signal, successively accesses the first signal generating means belonging to that block to identify the particular first signal generating means which has output the first signal."

Independent claim 4 differs from claim 1 in that in feature F2 there is a program counter for outputting a memory address signal in synchronism with the timing signal, the generating circuit for which has been

deleted. In addition, after feature F3, there is a specifying means for specifying some of the external signal input terminals as interrupt inputs. The end of feature F4 is amended to define that a signal on only one (instead of any) of the terminals in the group generates an interrupt.

II. The opposition division held that the grounds for opposition mentioned in Article 100(a) EPC did not prejudice the maintenance of the patent as granted, having regard inter alia to the following documents:

D1: Siemens Catalog ST 52, Section B, 1985: "SIMATIC S5 S5-115U Programmable Controller".

D2: EP-A-0 104 545

D3: Datenverarbeitung mit Mikroprozessoren, Teil 1: Hardware, R. Bodo, Hanser Verlag, München, Wien, 1983, pages 175 to 176, 215 to 235, and 292 to 294.

III. The opposition division reasoned as follows:

(a) in the summons to oral proceedings dated 29 May 1996:

"4) D1 discloses a programmable controller arrangement which either explicitly or implicitly contains all of the features F1-F3 of claim 1. Furthermore, in D1 (page 8/4, third paragraph) it is mentioned that, if certain events occur or certain input

signals change, cyclic program processing is interrupted. However, no details are given as to how such an interrupt arrangement could be organised, nor is it suggested that the system could be given the capability of distinguishing between interrupts received at different groups of terminals of a given input module."

(b) in the decision under appeal:

"6.2) The Opposition Division is of the opinion that the system of D3 establishes the source of an interrupt signal by way of a procedure involving the exchange of information on the data bus between the CPU and both the master and slave interrupt units, as well as the exchange of information on the three cascade lines (CAS 0 to CAS 2) linking the master and the slave interrupt units. As part of this procedure it is considered that the following steps are carried out:

a) An interrupt request (IR) is received by a slave interrupt unit;
b) The slave interrupt unit sends an IR to the master interrupt unit;
c) The master interrupt unit sends an IR to the CPU;
d) The CPU sends an interrupt acknowledge to the master interrupt unit;
e) The master interrupt unit again sends an IR to the CPU (together with a first byte);

f) The master interrupt unit sends an IR to the CPU one more time (together with a second byte);
g) The first and second bytes constitute the address of the interrupt routine to be executed by the CPU (and thus implicitly identifies the origin of the IR)."

"6.3) It is considered that this complex procedure would not give a hint to the skilled man to develop the relatively simple hierarchical access arrangement defined in feature F8 of claim 1 of the patent; namely [...]"

"7.2) The Opposition Division is of the opinion that the arrangement of D2 does not render claim 1 of the patent obvious, for the reasons given below;

a) The arrangement of D2 uses a single common interrupt line 19 to transmit an interrupt from the said external input/output boards 13 to the CPU 1 (see page 2, lines 13 to 18 and page 7, lines 2-8).
b) On receiving the interrupt the CPU 1 sends a common address to each of the said external input/output boards via the address bus 15 (see figure 3 and page 7, lines 10-20).
c) Each external input/output board 13 responds to this common address by sending an identification signal (namely, an

interrupt request identifying signal) to the CPU 1 on the data bus 17. This identification signal comprises one reserved bit for each external input/output board, by means of which each external input/output board can signal whether or not it initiated the interrupt (see page 3, lines 22-25; page 7, line 20 to page 8, line 7; and claim 1, lines 19-24).
d) [...] There is thus no hint in the disclosure of D2 of the hierarchical access arrangement defined by feature F8 of claim 1 of the invention; namely [...]"

IV. The appellant (opponent) lodged an appeal against the decision, paid the prescribed fee and filed a statement of grounds of appeal in time. The appellant requested that the decision under appeal be set aside and that the patent be revoked. In a letter of reply the respondent (proprietor) requested that the appeal be dismissed and that the patent be maintained as granted. As an auxiliary request, the respondent requested oral proceedings.

V. In a communication accompanying the summons to oral proceedings dated 13 October 1998 the Board expressed its preliminary opinion.

The appellant on 2 November 1998 filed a response and new documents (listed below), as evidence of the common knowledge of the skilled person.

Elektronik, Sonderheft 1, Mikroprozessoren hardware,

pages 107 to 112, Franzis-Verlag, 1977; D. Hammer: "Interruptverarbeitung bei Prozeßsteuerungen",

and from the same source on page 90; M. E. Lösel: "Die Interruptstruktur des Mikroprozessors F8".

The respondent also filed a reply, received 16 November 1998, which included new claims 1 and 4 of an auxiliary request, which adds to the end of feature F4 of claim 1 and the corresponding feature in claim 4 the wording:

"wherein the signal is latched until it is accessed at the terminal".

VI. Oral proceedings took place before the Board on 1 December 1998, during which the appellant requested that the new documents be admitted into the proceedings, whereas the respondent requested this be refused.

VII. During the course of the appeal, the appellant argued as follows:

The new documents were relevant, and as they represented common knowledge of the skilled person could be admitted even at so late a stage of the proceedings.

In order to determine which I/O board issued the interrupt, the system of D2 must have operated sequentially as claimed because, as is well known, in a microprocessor all processing actions were carried out in sequence and not simultaneously. Furthermore, in the system of D2 the ID-bits could not have been output from all I/O boards simultaneously because this would have led to bus contention if the same bit position from different boards had a different logic level. Thus the bit pattern containing the ID-bits must have been read, and therefore accessed, from each I/O board in separate read cycles, ie. successively. The separate bit patterns would then have been ORred together to form the final pattern described in D2. Even if this process was not explicitly described in D2, the skilled person would have realised that this was what was meant. The idea of grouping the interrupts into a hierarchy was obvious from the skilled person's common knowledge.

The cascaded structure of Programmable Interrupt Controllers (PICs) shown in the circuit on page 235 of D3 was a hierarchical structure because it had a number of slave PICs, corresponding to the groups, each connected a single master PIC, corresponding to a block. The description, starting at page 224 of D3, of the mechanism by which an interrupt at an input to a slave PIC was identified (see paragraph III above) was equivalent to successively accessing the second signal means (master PIC) and then the first signal means (slave PIC) as claimed. Although D3 only showed one master PIC (block), it would have been obvious to expand the system to include additional master PICs.

Finally, the claimed successive accessing of a signal generating means after an interrupt was nothing more than the well known technique of polling. The skilled person would therefore have considered polling the input interrupts in D1 to determine the source of the interrupt. However, it would not have made sense in the context of the modular system of D1 to poll all of the maximum possible 512 inputs disclosed on page 2/1, and this would have suggested polling the inputs according to the existing hierarchy of the inputs, namely in the order of cards (blocks) and then groups.

VIII. The respondent argued as follows:

The new documents were filed only one month before the oral proceedings which was too late for his Japanese client to arrange a translation and consider their content. Moreover, according to established jurisprudence of the boards of appeal, they should only

be admitted if they were prima facia relevant, which did not appear to be the case.

The prior art technique of polling was simply the process of checking each input to see if a signal was present. This was a slow process and the invention improved the speed by using an interrupt and then polling to find the source of the interrupt, a combination which was previously not known in the art. This differed from the prior art of D2 and D3 in that the processor was active in determining the interrupt and it did not simply wait for an address. As a result, the number of interrupts that could be serviced by the sequence controller of the invention was not limited by the width of the data bus which carried the address as it was in D2 or D3.

Apart from the above differences, the invention was faster than the prior art polling and simpler than the parallel systems of D2 and D3.

The invention was made in 1986 when it was not envisaged that sequence controllers would have so many interrupt sources. There was therefore no reason for the skilled person to consider solving the problem of servicing these interrupts in a way other than that described in the prior art and certainly not as claimed.

IX. The appellant requested that the decision under appeal be set aside and that the European patent No. 285 667 be revoked.

The respondent requested as main request that the appeal be dismissed, as first auxiliary request that the decision under appeal be set aside and that the patent be maintained with claims 1 and 4 as submitted on 16 November 1998 and otherwise as granted, and as second auxiliary request that it be afforded an opportunity to submit further amendments.

Reasons for the Decision

1. The appeal complies with Article 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. *Late filed documents*

2.1 The appellant sought to strengthen his view on what was considered as common general knowledge in the art by means of the late filed documents. The Board however sees no need to take these documents into account. As pointed out by the respondent, according to established jurisprudence, the minimum requirement for admissibility in appeal proceedings is that they are prima facia highly relevant. The Board agrees with the respondent that they are not and accordingly decides not to admit them under Article 114(2) EPC (cf. T 85/93, OJ EPO 1998, 183).

3. *Inventive step (main request)*

3.1 The patent concerns the problem of identifying in a sequence controller a signal input terminal that produced an interrupt. This is solved by grouping the

terminals into multiple blocks and subdividing the blocks into multiple groups each containing multiple terminals. When an interrupt occurs, it is identified by first checking the blocks in sequence to find the associated interrupt signal, and then checking the groups. Claim 1 defines that this checking is carried out by an access means which "successively accesses" signal generating means associated with the blocks and the groups.

3.2 It seems to the Board that the majority of the appellant's arguments was devoted to establishing that the claimed successive accessing to find the source of the interrupt was equivalent to "polling" and was common general knowledge in the art. The Board is of the opinion, already expressed at paragraph 6.11 of the Board's communication of 13 October 1998, that this is indeed the case and that device polling after an interrupt is an alternative to the other well known interrupt handling technique, proposed in D2 and D3, namely the vectored interrupt which the respondent contested.

3.3 However, as pointed out above, the invention is not simply device polling to determine the source of an interrupt, but its application to a two-level hierarchy of interrupts in order to avoid polling all of the interrupts. The Board agrees with and has essentially nothing to add to the opposition division's analysis of the prior art and its conclusion that none of the available prior art documents suggests this idea (see paragraph III above). In the following paragraphs the Board, however, presents its comments on the

appellant's new arguments.

3.4 The Board agrees with the opposition division's statement at paragraph 4 of the summons to oral proceedings (see paragraph III above) that D1 gives no details whatsoever of the interrupt mechanism, save that the user program can be interrupt driven. The Board considers that the appellant's attempt to read into D1 a hierarchical polling technique to mirror the structure of the inputs on the I/O cards is a clear case of using hindsight for which there is no indication in D1 or any other document. Rather, it appears to the Board that the skilled person would, using the above mentioned common general knowledge in the art, consider polling all the inputs in turn and, if that was too slow, using a vectored interrupt as in D2 or D3.

3.5 As far as D2 is concerned, the Board sees no indication of any hierarchy. Moreover, as mentioned above, the Board considers that D2 uses the principle of vectored interrupts rather than polling. Nor does the Board agree with the appellant that D2 discloses anything which falls under a literal interpretation of the claimed successive accessing. Whilst it is agreed that the interrupt processing itself may occur in successive steps corresponding to machine cycles of the microprocessor, the Board understands the reading of the byte formed by the ID-bits to be a single operation which occurs only once for each interrupt. Since only one bit from each I/O board is connected to the data bus, the Board cannot see how the data from different boards can conflict as argued by the appellant.

3.6 Despite the fact that the arrangement of D3 also uses the principle of vectored interrupts, the Board agrees with the appellant that, in this case, the process of extracting the interrupt address is technically speaking a successive accessing of the PICs which could thus fall under an interpretation of this feature of the claim taken in isolation. However, the claim also states that the successive accessing is applied in turn to the second and then the first signal generating means until it finds the particular one that has produced the interrupt. In other words the claim implies an element of querying various possible sources of the interrupt until it finds the correct one. The successive accessing in D3 however does not contain this element, but always yields the address of the interrupt after a fixed number of accesses.

3.7 In this respect, the Board would modify the opposition division's summary of the operation of D3 (see paragraph III above) by adding that the address of the interrupt is contained in the second and third bytes of a three byte sequence. Furthermore D3 discloses at page 227, lines 3 to 7, that in the cascade arrangement, the slave PIC outputs the two address bytes. However, nothing turns on these differences, since the address is still delivered in a fixed number of bytes.

3.8 Thus although the successive accessing in D3 results in the identification of the interrupt source, the Board considers that the claim specifies that the identification is to be done in a different way;

essentially reflecting the difference between device polling and vectored interrupts.

3.9 Finally, the Board does not agree with the appellant that it would be obvious to expand the systems to include additional master PICs (blocks) because D3 states in the second sentence in the last paragraph on page 226 that only one PIC can be used as a master.

3.10 Apparatus claim 4 is subject to the same observations, *mutatis mutandis*, as claim 1.

4. Since granted claim 1 involves an inventive step, it follows that the patent may be maintained as granted and it is not necessary to consider the respondent's auxiliary requests.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer P. K. J. van den Berg