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D E C I S I O N
of 26 September 2001

Case Number: T 0105/97 - 3.4.3

Application Number: 89200352.6

Publication Number: 0382948

IPC: H01L 23/50

Language of the proceedings: EN

Title of invention:
Supply pin rearrangement for an integrated circuit

Applicant:
Koninklijke Philips Electronics N.V.

Opponent:
-

Headword:
Integrated circuit module/PHILIPS

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
-

Decisions cited:
-

Catchword:
-

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Case Number: T 0105/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 26 September 2001

Appellant: Koninklijke Philips Electronics N.V.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 14 August 1996 refusing European patent application No. 89 200 352.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. J. Vogel

Summary of Facts and Submissions

1. European patent application No. 89 200 352.6 was refused in a decision of the examining division dated 14 August 1996. The reason for the refusal was that the claims according to applicant's requests did not meet the requirements of Articles 123(2) and 84 EPC.

II. The reasoning in the decision can be summarized as follows:

(a) The independent claims directed respectively to an integrated circuit module and to an integrated circuit chip contain the following features which have been generalized from the specific features disclosed in the application as filed, contrary to the requirements of Article 123(2) EPC:

(i) The feature specifying first and second supply pins connected to first and second supply voltages different from each other is only disclosed in conjunction with Figures 2 and 4 which show *two* pairs of supply pins arranged opposite to each other. The independent claims on the other hand specify only one pair of supply pins.

(ii) The feature defining a first and a second output pin to be next to the first and second supply pin, respectively, is only disclosed in the context that the conductive connection between the output pins and the respective bonding pads of the integrated circuit chip are arranged adjacent to the respective connection of the supply pins.

(iii) Moreover, the disclosure refers only to a module, i.e. the complete structure comprising pins and bonding pads at specific locations. A complete module defining short output path lengths has to incorporate the definitions of output buffers near the respective output pads and supply voltage pads.

(b) As to Article 84 EPC, claims relating to an integrated circuit module only specify the arrangement of the pins of the module but leaves open whether the contact pads of the chip have a corresponding arrangement or not. It is therefore not clear how the aggregated electrical path lengths for the power supply and output interconnections can be formed as the shortest possible interconnections.

(c) Although an objection of lack of inventive step was not a ground for the refusal, the examining division was also of the opinion that the claimed subject matter did not involve an inventive step having regard to the prior art documents

D1: EP-A-0 205 728;

D2: Patent Abstracts of Japan, vol. 8, No. 272 (E-284) [1709], 13 December 1984 & JP-A-59-144 155;

D4: Patent Abstracts of Japan, vol. 10, No. 325 (E-451) [2381], 6 November 1986 & JP-A-61-133 651; and

D5: Computer Design, vol. 25, No. 21, 15 November 1986, pages 28 to 32.

According to the decision, the claimed device differs from that of document D1 only in that output pins are put adjacent to the supply voltage pins. This is an obvious measure, since, firstly, the adjacent pins are called "I/O pins" in document D1, and secondly, document D5 shows the provision of pins dedicated exclusively to the output of signals next to centrally arranged supply voltage pins. Documents D2 and D4 also disclose an arrangement of centrally positioned, adjacent voltage supply pins.

III. The appellant (applicant) lodged an appeal on 11 September 1996, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 19 December 1996 together with new claims.

IV. At the oral proceedings held on 26 September 2001 the appellant filed new application documents and requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 10 filed during the oral proceedings;

Description: pages 2, 2a, 3, 4a, 4b filed during the oral proceedings,
pages 1, 5 to 10, as originally filed;

Drawings: Sheets 1 to 3, as originally filed.

V. The independent claims 1 and 7 according to the appellant's request read as follows:

"1. An integrated circuit module comprising

- an integrated circuit chip (300) comprising a memory matrix;
- a plurality of external connection pins (1, 2, ..., 24), comprising at least a first supply voltage pin for connection to a first supply voltage (V_{cc}) and a second supply voltage pin (7) for connection to a second supply voltage (GND) different from the first supply voltage (V_{cc}), the first supply pin and the second supply pin being located adjacent one another;
- a plurality of conductive connections (322, 324, ...) coupling the integrated circuit chip (300) to the external connection pins (1, 2, ..., 24), an aggregate electrical path length of each of said supply pins and the respective conductive connection between the integrated circuit chip and the supply pin being equal to or shorter than an aggregate electrical path length of any of the connection pins, not being a supply pin, and the respective conductive connection between the circuit and the relevant connection pin not being a supply pin;

characterized in that the external connection pins comprise output pins (5, 8), and the integrated circuit chip (300) comprises respective output buffers connected to output pins for supplying respective output signals, a respective one of the output pins being located next to each of the first and second supply pins."

"7. An integrated circuit chip comprising a memory

matrix having a series of bonding pads for connection to connection pins, wherein the bonding pads comprise a first supply pad (316) for receiving a first supply voltage (V_{cc}), a second supply pad (314) for receiving a second supply voltage (GND) different from the first supply voltage; the first and second supply pads being located next to each other in the series; characterized in that the series of bonding pads contains output pads, the integrated circuit chip comprising output buffers coupled to respective ones of the output pads for supplying output signals, a respective one of the output pads being located in the series next to each of the first and second supply pads."

VI. The appellant presented essentially the following arguments in support of his request:

(a) Claim 1 defines the aggregate electrical path length related to the supply pins to be equal to or shorter than an aggregate electrical path length of any other connection pin. This feature is well-defined and has the effect of reducing the electromagnetic interferences to other parts of the integrated circuit module. Although the skilled person usually would arrange the bonding pads of the integrated circuit chip in the same order as the connection pins, this is not necessary for reducing the electromagnetic interference.

(b) Document D1 relates to a different type of device (CCD device) than the memory devices disclosed in the application in suit. The device of document D1

requires two different voltage supplies and addresses the problem of electromagnetic radiation emitted which may interfere with other neighboring device, i.e. a problem entirely different from that addressed by the application in suit. The teaching of document D1 was thus not relevant for reducing the inductive effect.

Reasons for the decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and Clarity (Articles 123(2) and 84 EPC)*

2.1 Claim 1 contains features of claims 1, 3, 7, and 9 as filed and further specifies that (a) the first and second supply voltages (VCC, GND) are different from each other; (b) the chip comprises output buffers; and (c) the first and second output pins are next to the first and second supply pins, respectively.

Independent claim 7 is based on the embodiments of Figures 2 and 4 and also contains the features (a) to (c).

2.1.1 In the decision under appeal, the examining division objected against feature (a) under Article 123(2) EPC, since the only clear disclosure regarding the first and second voltages being different from each other was in the embodiments of Figures 2 and 4, which show **two** pairs of such first and second supply voltage pins. In the claims under consideration in the decision under

appeal, however, only one pair of supply voltage pins was specified.

The Board is however of the opinion that the labelling "VCC" and "GND" of the supply voltage pins clearly indicate that the first and second supply voltages are different from each other. Furthermore, Figures 2 and 4 show only a preferred embodiment with two pairs of supply voltage pins, whereas claim 1 as filed only specified one pair of supply pins.

2.1.2 As to feature (b), output pins on both sides of the supply pins which are connected to on-chip output buffers are disclosed on page 8, lines 13 to 16 in conjunction with Figure 2.

In the decision under appeal, the examining division had objected against the introduction of output pins and output pads without any reference to the corresponding output buffers. Independent claims 1 and 7 refer to output buffers, so that this objection has been met by the amended claims.

2.2 An objection under Article 84 EPC was raised in the decision under appeal, since claim 1 only defined the arrangement of the pins of the module without specifying that the contact pads of the chip have a corresponding arrangement. It was therefore not clear how the aggregated electrical path lengths for the power supply and output interconnections could be the shortest possible path lengths.

The appellant has however convincingly argued that the scope of claim 1 is clearly defined by the requirement that the aggregate electrical path length of each

supply pin and the respective conductive connection between the integrated circuit chip and the supply pin is equal to or shorter than an aggregate electrical path length of any other connection pin which is not a supply pin. Moreover, claim 1 as filed does not contain any feature defining the arrangement of the contact pads of the integrated circuit chip with respect to the arrangement of the contact pins of the module, so that support for the present formulation of claim 1 exists in the application as filed.

2.3 Therefore, in the Board's judgement, the requirements of Articles 84 and 123(2) EPC are met.

3. *Novelty and inventive step (Articles 54 and 56 EPC)*

3.1 The application in suit relates to integrated circuit chips comprising a memory matrix and integrated circuit modules comprising such integrated circuit chips. The technical problem addressed in the application as filed relates to the occurrence of parasitic voltage fluctuations, a problem which becomes more severe with increasing miniaturization and switching speed.

The present invention solves this problem by suggesting two measures: (i) In the integrated circuit module, the supply pins VCC and GND should be put adjacent to each other and so that the aggregated conductive path to the chip is shorter than the conductive path of any other pins to the chip; and (ii) the output pins should be placed next to the power pins, i.e. the output pins have the next shortest connection to the chip. For the integrated circuit chip, such an arrangement is optimized when the bonding pads for the supply voltages are arranged adjacent to each other and bonding pads

for the output signals are arranged adjacent to the supply voltage bonding pads.

3.2 Document D1 discloses an integrated circuit chip module for a CCD integrated circuit chip powered by two different supply voltages (VCC and VDD) and a common ground GND (cf. Figure 2). Due to rapid internal switching of the power supply in such an integrated circuit, electromagnetic radiation from the integrated circuit chip tends to adversely affect the operation of other electronic components in the vicinity (cf. page 1, lines 10 to 24). In order to limit the radiated energy, it is suggested in document D1 to place the power supply pins 10, 11, 12 adjacent to each other with the ground pin in the middle position, so that the current path of the voltage supply current to and from the integrated circuit chip is minimized (cf. page 4, lines 3 to 16).

Document D1 does not provide any teaching as to the function of the pins other than the voltage supply pins 10, 11, 12, since all pins 8 to 21 of the module are generally termed "I/O pins" (cf. page 3, lines 21 to 33). Thus, there is no specific teaching regarding the location of the output pins.

3.2.1 The device of claim 1 differs from that of document D1 in that (i) the integrated circuit chip comprises a memory matrix, whereas the integrated circuit chip in the device of document D1 is a CCD device; and that (ii) first and second output pins are located next to a respective one of the first and second supply pins, whereas in document D1 there is no disclosure regarding the position of the output pins.

3.2.2 The device of independent claim 7 differs of document D1 in that (i) the integrated circuit chip comprises a memory matrix, whereas the integrated circuit chip in the device of document D1 is a CCD device; and that (ii) first and second output pads are located next to a respective one of the first and second supply pads, whereas in document D1 there is no disclosure regarding the position of the output pads.

3.3 Document D5 discloses a pin layout for integrated circuit modules which provides a reduced parasitic inductance with respect to conventional integrated circuit modules (cf. page 30, section "Attacking the problem"; page 32, Figure). The proposed solution for a dual in-line module is to place the VCC and GND pins on opposite sides at the center of the module, and to use extra GND pins adjacent to each other. The output pins are located adjacent to the GND pins.

3.3.1 Thus, the device of claim 1 differs from that of document D5 in that (i) it relates to a module for an integrated circuit chip comprising a memory matrix, whereas the modules described in document D5 relate to advanced CMOS logic integrated circuits; (ii) output pins are located adjacent to the two voltage supply pins; and (iii) the two voltage supply pins are located adjacent to each other.

3.3.2 Similarly, the device of independent claim 7 differs from that of document D5 in that (i) the integrated circuit chip comprises a memory matrix, whereas integrated circuit chip modules described in document D5 relate to advanced CMOS logic integrated circuit chips; (ii) output pads are located adjacent to the two voltage supply pads; and (iii) the two voltage supply

pads are located adjacent to each other.

3.4 Document D2 discloses integrated circuit packages each having two pairs of first and second supply voltage pins adjacent to each other and the two pairs being located on opposite sides of the package (cf. abstract). The purpose is to provide symmetrical arrangement of the connection pins in order to shorten the wiring between adjacent integrated circuit packages. Through this arrangement, however, the output pins/pads cannot be located adjacent to each of the first and second supply pins/pads, as required in independent claims 1 and 7.

3.5 Document D4 teaches to assign the power source line (VCC) to the connection pin having the shortest path length to the integrated circuit chip in order to reduce power source noises (cf. abstract). In contrast to the claimed device, however, document D4 neither specifies the location of the other voltage supply pin (GND) nor the location of the output pins.

3.6 Thus, the subject matter of independent claims 1 and 7 is new.

3.7 In the decision under appeal, document D1 was considered to represent the closest prior art. Independent claims 1 and 7 as amended specify an integrated circuit chip which comprises a memory matrix, whereas the device of document D1 relates to a CCD device.

3.7.1 As convincingly argued by the appellant, document D1 relates to a CCD device where the operation of the CCD device is controlled by high-frequency clock signals

which give rise to radiation of high-frequency electromagnetic waves adversely affecting the operation of external circuits (cf. page 1, lines 10 to 22). Document D1 thus aims to reduce the interference caused by the high-frequency electromagnetic radiation (cf. page 2, lines 14 to 31), a problem which does not occur in a memory matrix. Therefore, a skilled person seeking to solve the problem of reducing the parasitic inductive voltage fluctuation in a memory module would not consider document D1 to be relevant.

3.8 In view of the above considerations, document D5 is considered to be the closest prior art, since it relates to a similar type of devices (CMOS logic circuits) and addresses the same problem (reducing voltage fluctuations due to parasitic inductances) as that of the application in suit.

The above technical problem is however solved in document D5 by arranging the voltage pins on the opposite sides of the integrated circuit chip module and not on the same side as in the claimed device. Furthermore, the output pins are not adjacent to the voltage pins as specified in claim 1.

Similarly, document D5 teaches to arrange the supply bonding pads of the integrated circuit chip opposite to each other, and furthermore does not provide any teaching to move the output pads adjacent to the supply pads as specified in claim 7.

Since document D1 and D5 relate to different types of devices and to different problems associated with such devices, a combination of the teaching of documents D5 and D1 would not be regarded as obvious by the person

skilled in the art having regard to the problem addressed in the application in suit.

3.9 Therefore, in the Board's judgement, the subject matter of independent claim 1 and claim 7 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of

Claims: 1 to 10 filed during the oral proceedings;

Description: pages 2, 2a, 3, 4a, 4b filed during the oral proceedings,
pages 1, 5 to 10, as originally filed;

Drawings: Sheets 1 to 3, as originally filed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla