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D E C I S I O N
of 19 June 2001

Case Number: T 0044/97 - 3.5.2

Application Number: 86116058.8

Publication Number: 0231452

IPC: G07B 17/02

Language of the proceedings: EN

Title of invention:
Microprocessor systems for electronic postage arrangements

Patentee:
PITNEY BOWES INC.

Opponent:
Francotyp-Postalia Aktiengesellschaft & Co.

Headword:
-

Relevant legal provisions:
EPC Art. 56, 84

Keyword:
"Inventive step - yes (patent amended)"
"Clarity - unamended phrase not open to objection under Article 84 EPC in opposition or appeal proceedings)"

Decisions cited:
G 0009/91

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0044/97 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 19 June 2001

Appellant: (Proprietor of the patent)
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Decision under appeal: **Interlocutory decision of the Opposition Division of the European Patent Office posted 28 October 1996 concerning maintenance of European patent No. 0 231 452 in amended form.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
P. H. Mühlens

Summary of Facts and Submissions

I. The proprietor as sole appellant contests the interlocutory decision of the opposition division that whereas European patent 231 452 as amended in accordance with the proprietor's fourth auxiliary request met the requirements of the EPC, the proprietor's higher order requests were rejected.

II. The following prior art documents, which were among those considered in the first instance proceedings, featured in the appeal proceedings:

D1: EP-A-0 019 515

D2: GB-A-2 079 223

D7: CH-A-554 574

D10: EP-A-0 026 734

D11: DE-A-3 024 370

D12: P.G. Depledge et al.: "Fault-tolerant computer systems", IEE PROC. , vol. 128, part A, No. 4, May 1981, pages 257 to 272.

III. The appeal (see present single request below) is now essentially directed against the rejection of the proprietor's second auxiliary request. The reason given in the decision under appeal for rejecting this request was that the subject-matter of amended independent claim 7 of this request did not involve an inventive step in view of common general knowledge in the art in relation to redundant dual microprocessor systems, as

exemplified by D10 and D11, and the allegedly inevitable result of repairing such a system by replacement of one of the microprocessors.

IV. In a reasoned communication accompanying the summons to oral proceedings, the board expressed the provisional opinion that the decision under appeal appeared to be well founded as far as the rejection of the proprietor's main and first auxiliary request was concerned, but that the board was inclined to disagree with the inventive step argument on which the rejection of the proprietor's second auxiliary request had been based.

V. Following the debate at the oral proceedings held before the board on 19 June 2001, the appellant filed a single request - an amended form of the second auxiliary request rejected by the decision under appeal - replacing all previous requests.

VI. Independent claim 7 of the single request is now worded as follows:

"7. An electronic postage meter system having, a microprocessor (10), addressable and redundant nonvolatile memory means (20, 21), said nonvolatile memory means having two separate nonvolatile memory units (20, 21), a control bus having a plurality of control lines coupled to the microprocessor, an address bus means (22, 24) connected to said nonvolatile memory means and said microprocessor (10), and a data bus means (23, 25) connected to said nonvolatile memory means (20, 21) and said microprocessor (10), each memory unit being connected to different lines of said address bus and different lines of said data bus, so

that said random access memory units may be separately addressed, wherein:

said microprocessor (10) is programmed to generate data for sequentially writing to said nonvolatile memory means (20, 21) and to read data from said nonvolatile memory means (20, 21) such that said data is redundantly written in respective ones of said memory units; and

means are provided for causing said data to be stored in said respective nonvolatile memory units (20, 21) in different forms."

Claims 8 to 10 are dependent on claim 7.

VII. The appellant proprietor argued essentially as follows:

It was an essential feature of claim 7 that the data was stored redundantly in the two memories in different forms. The opposition division had accepted that the use of different codings was not suggested by the prior art and was therefore inventive, but had argued that another way of storing the data in different forms would be obvious. In particular, it had been argued that when replacing a defective memory unit by a spare produced by a different manufacturing process, a system falling within the terms of claim 7 would inevitably be produced, so that the claim would be obvious.

However no evidence had been produced that such a substitution ever took place before the priority date of the patent. In fact, servicing and repair of franking machines would only be carried out in practice by the original manufacturer or its authorised service

representative. When replacing a defective memory chip, the manufacturer would not select a new chip at random, but would select a component whose properties and characteristics corresponded as far as possible with those of the failed component. Accordingly it was extremely unlikely that in some accidental way a system according to claim 7 would have been produced by routine modification of the prior art systems. On the contrary, it was only after receiving the teaching of the present invention that a skilled engineer would have any incentive to install hardware such that data would be stored in different forms in the two memories.

The opposition division had confirmed that none of the relevant prior art documents D2, D7, D10, D11 or D12, taught the storage of redundant data using different codings. In the proprietor's view the same conclusion applied to the more general teaching of different forms. In particular, the opponent's argument based on D2 resulted from a misconstruction of the claim; the fact that in D2, under fault conditions, different data would be stored in the two memories had no relevance to claim 7 which, on its proper construction, required redundant storage of the same data in different forms.

VIII. The respondent opponent's arguments can be summarised as follows:

The reasoning and conclusion of the opposition division in the decision under appeal was correct. Amended claim 7 was unclear, because of the phrase "different forms" which could be given a very broad interpretation beyond the specific disclosure in the patent specification of "different codings". In its widest interpretation it was obvious in view of D2 which

showed two redundant memories deliberately arranged to be addressed by different gate circuits so that, under particular conditions the form of the data stored in the two memories would inevitably be different.

Even in the narrower interpretation of "different forms" as "different codings" the postage meter of claim 7 was obvious from the combination of either D1 or D2 with D7, cf D7, column 2, lines 18 to 31, in which there was an explicit teaching of increased security resulting from storing data redundantly with different codings on a data card substrate and on an information record track formed on the card. Although the overt purpose of the dual coding in D7 was the detection of fraud, the person skilled in the art would appreciate that this technique would also be advantageous in detecting accidental corruption of data in a redundant memory system.

IX. The appellant proprietor requested that:

- the decision under appeal be set aside and that the patent be maintained in amended form on the basis of:

- claims 1 to 10;

- description, pages 2 to 6; and

- drawings, Figures 1 to 6;

all as filed in the oral proceedings of 19 June 2001.

X. The respondent opponent requested that the appeal be dismissed.

Reasons for the Decision

1. The appeal is admissible.

2. Since the proprietor is sole appellant, claims 1 to 6 are protected against *reformatio in peius* of the decision of the opposition division; only claims 7 to 10 and the amended description are to be examined by the board.

3. *Permissibility of the amendments*

3.1 The amendments made to the claims and description of the patent after grant comply with the requirements of Articles 76(1) and 123(2) and (3) EPC. In particular independent claim 7, which, in its granted form, had been objected to in the opposition on the ground specified in Article 100(c) EPC, now includes the features of "a control bus having a plurality of control lines coupled to the microprocessor" and "each memory unit being connected to different lines of said address bus and different lines of said data bus, so that said random access memory units may be separately addressed". The omission of the latter feature had been objected to as extending beyond the content of the earlier application as filed. In addition dependent claims 10 to 12 as granted have been replaced by new claim 10 which corresponds to the passage at column 3, lines 48 to 51 of the description of the granted patent which in turn is identical to the passage at page 6, lines 13 to 15 of the parent application as filed.

3.2 *Clarity*

The respondent opponent objected to an alleged lack of clarity in the wording of the feature "means are provided for causing said data to be stored in said respective nonvolatile memory units in different forms" in amended claim 7 as likely to give rise to difficulty in determining the scope of protection, in particular as regards the range of the phrase "different forms" compared to the described embodiment of "different codings". However, as the board pointed out in the oral proceedings, the wording objected to was that of claim 7 as granted and as such not open to objection under Article 84 EPC in opposition or appeal proceedings, lack of clarity not being a ground for opposition. The power of an opposition division or a board of appeal to examine claims amended in opposition or appeal proceedings in that respect was only a power to examine the amendments; see the decision of the Enlarged Board of Appeal G 9/91 OJ EPO 1993, 408, reasons 19.

4. *Novelty*

Novelty of the subject-matter of the independent claim 7 is not in dispute.

5. *Inventive step*

5.1 Claim 7 differs from claim 1 *inter alia* in that it does not specify that the microprocessor is directly connected to each of the address and data lines and thus covers not only the single microprocessor/dual memory embodiment of Figure 1 but also the full dual microprocessor system of the embodiment of Figure 6. Having regard to the protected status of claim 1 it

appears expedient to the board to regard claim 7 as the disjunction of two notional claims directed to the Figure 1 and Figure 6 embodiments respectively according as to whether the direct connection (as specified in claim 1) is present or not. Since the first of these notional claims then is equivalent to claim 1 with the additional feature that "means are provided for causing said data to be stored in said respective nonvolatile memory units in different forms", the argumentation of the opposition division underlying its finding that claim 1 involved an inventive step (see decision under appeal, points 24 to 28) applies *a fortiori* to this first branch of the disjunction. Putting it another way, this notional part of claim 7 is effectively dependent on claim 1 and has the same protected status.

5.2 As regards the second notional part of claim 7, the opposition division concluded that no inventive step was involved and the respondent opponent supports this view. It is indeed hardly deniable that the feature of separate address lines has little weight in assessing inventive step in a full dual microprocessor system of the kind shown in Figure 6 of the patent, given that full dual systems with each processor having its respective address bus connection to its respective memory are undisputedly common general knowledge in the broad art of redundant computer systems (cf D10, D11, D12) and that the application of such a standard technique for enhancing reliability to the field of electronic postage meters would appear to have been a routine consideration for a person skilled in the latter art.

5.3 However, part of the reasoning in the decision under

appeal at point 19 is based on a scenario postulated by the opposition division according to which one of the two memory units in the obvious full dual system would fail and be replaced by a non-matching unit thus "inevitably" producing a system in which "means are provided for causing said data to be stored in said respective nonvolatile memory units in different forms".

5.4 The board agrees with the appellant's questioning of the legitimacy of this latter part of the argument. An allegation that the skilled person would inevitably produce a postage meter accidentally identical to the claimed meter in the course of solving an unrelated problem, ie performing a routine repair, is indeed misconceived as an inventive step argument in the present context. It ignores entirely the relevant problem which is further to enhance the reliability of a postage meter comprising a redundant microprocessor system with separate address lines (patent, column 4, lines 43 to 50). The speculation that a repair man might *faute de mieux* replace a broken memory by a different type does not even begin to provide a suggestion that a skilled person addressing the problem of enhancing reliability would deliberately arrange for data to be stored in the different memories in different forms which difference would be exploitable to overcome the effects of transients affecting both units of a redundant dual system. In this context it is appropriate to quote the passage at column 5, lines 31 to 35 of the patent specification:

"It will, of course, be understood that the programs of the microprocessor have appropriate subroutines to determine, if a comparison between the data shows an

inconsistency, which memory bears the greater likelihood of correctness."

5.5 Neither is the board persuaded by the respondent opponent's argument that D2 teaches, albeit in a system with common address lines, means for causing data to be stored in said respective nonvolatile memory units (20, 21) in different forms as specified in claim 7. It is true that the memory input circuitry in D2 is deliberately so arranged that different integrated circuit packages are involved for the respective memory data inputs which under fault conditions would lead to data being stored in different forms, but only in the sense that the memories would store different data as a result of a fault in one of the redundant duplicate inputs. This is not the same as the claim 7 arrangement in which the same correct data is stored redundantly in deliberately different forms in the fault-free condition. A good-faith purposive construction of the phrase "different forms" in claim 7 requires that the different forms are exploitable further to enhance the reliability provided by redundant separately addressed memory units as explained in the paragraph above. This in turn requires that the same data is stored in different forms in normal fault-free operation.

5.6 As regards the argument based on D7, nothing has been said on appeal which casts any doubt on the refutation of this argument at point 20 of the decision under appeal, penultimate paragraph. D7 addresses a different problem (fraud) in a different field (credit cards). The link to the problem of enhancing postage meter reliability is too remote for the person skilled in the latter art realistically to be regarded as deriving inspiration from the teaching of D7.

5.7 In effect the board agrees with the conclusion of the opposition division in the decision under appeal that amended claim 7 involves an inventive step on the "different codings" interpretation of "different forms", but sees no basis either in the EPC or the prior art for objecting to the latter unamended phrase.

6. The description and dependent claims have been adapted to the present claims. The prior art according to D2 has been acknowledged in the amended description of the patent.

7. The board judges that, taking into consideration the amendments made by the proprietor during the appeal proceedings, the patent and the invention to which it relates meet the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to maintain the patent as amended in the following version:

- claims 1 to 10;

- description, pages 2 to 6; and

- drawings, Figures 1 to 6;

all as filed in the oral proceedings of 19 June 2001.

The Registrar: The Chairman:

M. Hörnell W. J. L. Wheeler