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D E C I S I O N
of 10 October 2001

Case Number: T 1083/96 - 3.4.3

Application Number: 89110480.4

Publication Number: 0353426

IPC: H01L 23/52

Language of the proceedings: EN

Title of invention:
Semiconductor integrated circuit device comprising conductive layers

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
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Case Number: T 1083/96 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 10 October 2001

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 31 July 1996 refusing European patent application No. 89 110 480.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
J. Van Moer

Summary of Facts and Submissions

I. European patent application No. 89 110 480.4 was refused by the decision of the examining division dated 31 July 1996. The ground for the refusal was that the subject-matter of claims 1 to 6 as filed with the letter dated 11 June 1996 did not involve an inventive step (Article 56 EPC) having regard to a combination of the prior art documents

D1: EP-A-0 246 458 and

D4: US-A-4 673 904

In the decision under appeal the examining division further observed that claim 5 and 6 were not clear (Article 84 EPC) and that their subject-matters extended beyond the content of the application as filed (Article 123(2) EPC).

II. Independent claim 1 on which the decision was based reads as follows:

"1. A semiconductor integrated circuit comprising:

a) a semiconductor body (21);

b) an insulation layer (10; 32) formed on said semiconductor body (21);

c) a first conductive wiring layer formed in said insulation layer (10; 32), containing a first signal wiring line (11; 42) for transmitting signals, and containing a first constant potential wiring line (13; 41, 43) held at a constant potential, where said first

constant potential wiring line (13; 41, 43) is disposed to extend in the lengthwise direction of said first signal wiring line (11; 42);

d) a second conductive wiring layer formed in said insulation layer (10; 32), arranged above said first conductive wiring layer, containing a second signal wiring line (12; 37, 33) for transmitting signals parallel to said first signal wiring line (11; 42) of said first conductive wiring layer, and containing a second constant potential wiring line (15; 44, 46) held at a constant potential, where said second constant potential wiring line (15; 44, 46) is disposed to extend in the lengthwise direction of said second signal wiring line (12; 37, 33) and vertically above said first constant potential wiring line (13; 41, 43) of said first conductive layer;

wherein

e) said first and second signal wiring lines (11; 42; 12; 37, 33) are used to transmit different signals, and

f) said first constant potential wiring line (13; 41, 43) of said first conductive wiring layer and said second constant potential wiring line (15; 44, 46) of said second conductive wiring layer are electrically connected vertically via a connection electrode (14; 47, 48) disposed to extend in the lengthwise direction of the signal wiring (11, 12; 33, 37, 42), thereby forming a wall configuration, and

g) said wall configuration is arranged between said first signal wiring line (11; 42) of the first conductive wiring layer and said second signal wiring

line (12; 37, 33) of the second conductive wiring layer."

III. The appellant (applicant) lodged an appeal on 27 September 1996. The appeal fee was paid on the same date. The statement setting out the grounds of appeal was filed on 29 November 1996.

IV. In response to a communication from the Board, the appellant filed with his letter dated 13 July 2001 amended claims 5 and 6 and new pages of the description.

V. The appellant requests that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 4 filed with the letter dated 11 June 1996
5 and 6 filed with the letter dated 13 July 2001

Description: pages 7 to 13 as originally filed
pages 1, 1a, 2, 4 and 5 as filed with letter dated 11 June 1996
pages 1b, 3 and 6 as filed with letter dated 13 July 2001

Drawings: Sheets 1/6 to 6/6 as originally filed

VI. In the decision under appeal the examining division argued essentially as follows:

- Document D1 represents the closest prior art. It discloses a semiconductor integrated circuit

comprising first and second wiring layers. Signal and constant potential wiring lines extending parallel to each other are alternately provided in each wiring layer. The constant potential wiring layers of both wiring layers are interconnected at regular intervals so as to form three-dimensional power planes which minimize cross-talk between the signal wiring lines. In the specific example shown in this document, the wiring lines of the first and second wiring layers extend orthogonal to each other.

- The circuit claimed in claim 1 of the patent in suit differs from this known device in that:

  (a) the signal wiring lines of the first and second wiring layer extend parallel to each other, and

  (b) the connection electrode between vertically connected constant potential lines extends in the lengthwise direction of the wiring lines so as to form a wall-like configuration.

- The objective problem associated with these features is the effective reduction of cross-talk between signal wiring lines which extend parallel to each other in vertically adjacent wiring layers but do not vertically overlie each other.

- The device as claimed, however, does not involve an inventive step for the following reasons:

  Feature (a) listed above merely concerns a design

option for the layout of signal wiring of integrated circuit devices. The teaching of document D1 is, however, not limited to a wiring layout in which the signal lines of vertically superposed wiring layers cross each other.

Feature (b) is obvious having regard to the basic physical principles underlying the electromagnetic shielding of conductive structures. A skilled person knows that an ideal shield requires a complete enclosure of a signal line with a constant potential structure. Practical constraints, however, do not allow such a complete shielding and a compromise is to be found, as shown in document D1 for wiring layers with signal lines extending in orthogonal directions. It would have been apparent to the skilled person that the vertical connections between the constant potential lines shown in document D1 could be extended in the lengthwise direction so as to form a wall-like configuration when the signal lines extend all parallel to each other. This assessment of the abilities and knowledge of a skilled person is confirmed by document D4 in which different shielding structures for parallel extending signal lines, including wall-like configurations, are disclosed.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments (Articles 84 and 123(2) EPC)*

2.1 Claim 5

In the decision under appeal, the examining division objected that claim 5 was not clear, since it did not specify the location and direction of extension of the third signal wiring line 52. Due to this unclear definition, the claimed structure includes circuit structures different from those disclosed in Figures 9 and 12 of the application in suit, contrary to Article 123(2) EPC.

In the amended claim 5, it is specified that the wiring lines of the third conductive wiring layer are parallel to the wiring lines of the second conductive layer. It is, therefore, clear that the wiring lines of all three layers are parallel to each other as disclosed by Figures 9 to 12 of the application in suit.

2.2 Claim 6

It was further objected in the decision under appeal that the phrase "disposed in opposition to" used in claim 6 was not clear for defining the specific location of the further constant potential wiring lines 56 and 57. This lack of clarity of the claim also raised an objection of undisclosed subject-matter.

This claim has been amended to state that the "further constant potential wiring line (56, 57) in said second conductive wiring layer being disposed **with respect to** (in opposition to) said second constant potential wiring line (44, 46) **so that** (with) said second signal wiring line (33,37) of said conductive wiring layer **is** () set at the center therebetween" (the previous wording is placed between parentheses for the ease of

comparison). It is, in the Board's view, clearly specified that the signal wiring line is located between the two constant potential lines, as shown in Figure 12 of the application in suit.

2.3 The Board is, for these reasons, satisfied that the amendments made to present claims 5 and 6 overcome the objections raised by the examining division.

3. *Inventive step (Article 56 EPC)*

The only remaining issue in the present appeal is that of inventive step.

3.1 It is not in dispute that document D1 represents the closest prior art.

This document relates to a module for packaging semiconductor chips on a substrate and addresses the problem of efficient power distribution and high quality signal transmission (i.e. minimal cross-talk between signal lines) to the chips. The disclosed module contains first and second wiring layers embedded in insulation layers (11, 21, 27), provided in different planes. The first wiring layer includes ground (17), power (16) and signal lines (19, 20) with at least one power or ground line located between coplanar signal lines to minimize cross-talk between these signal lines. The second wiring layer contains further signal wiring lines 19 and 20 and constant potential wiring lines 16 and 17, the latter being interspersed with the signal wiring lines 19 and 20. To facilitate efficient power distribution, the power lines of the same voltage belonging to different wiring layers are interconnected to form a three dimensional

structure. Although the wiring lines in each plane run parallel to one another, the wiring lines in different planes are orthogonal with respect to one another (cf. column 4, lines 11 to 24; column 5, lines 31 to 40; column 16, lines 31 to 53; column 19, lines 1 to 15; column 20, lines 53 to 57; Figures 1, 12 and 13).

3.2 The device claimed in claim 1 of the application in suit differs from the one disclosed in document D1 in that:

(a) it is a semiconductor integrated circuit and not a module for packaging semiconductor integrated circuit chips;

(b) the signal wiring lines and the constant potential wiring lines belonging to different, vertically superposed wiring layers run parallel to each other;

(c) two constant potential wiring lines belonging each one to a different, vertically superposed wiring layer are located above one another;

(d) the two constant potential wiring lines are vertically connected via a connection electrode which extends in the lengthwise direction to form a wall configuration; and

(e) the wall configuration is arranged between the two signal wiring lines.

3.3 In view of the above distinguishing features, the objective problem addressed by the invention is to prevent signal interference between wiring lines in

different wiring layers in a semiconductor integrated circuit device with a relatively high degree of integration. This is also the problem stated in the application in suit (cf. the published application column 1, lines 1 to 3 and column 1, line 52 to column 2, line 3).

3.4 In the decision under appeal, the examining division argued that the fact that in document D1 the wiring lines in different wiring layers are orthogonal to each other is merely a design option for the layout of integrated circuit devices.

However, the Board concurs with the appellant in that document D1 clearly states that an orthogonal wiring arrangement is highly desirable, since the formation of a three dimensional square hatched meshed plane by the power lines achieves extremely low inductance, low capacitance and low resistivity, providing therefore an optimum shielding effect against cross-talk (cf. D1, column 5, lines 35 to 40 and column 19, lines 1 to 8). The arrangement of the wiring layers shown in this document's embodiment is, therefore, not merely a design option, but constitutes an essential aspect of the chip packaging structure disclosed in this document.

3.5 Document D4 discloses a support substrate for interconnecting electronic components comprising only a single wiring layer. The conductors, extending in parallel to each other, are provided with a conducting shield to avoid cross-coupled interference (cf. D4, Abstract). The shielding structures which are shown in Figure 2 of this document comprise a shield completely surrounding the conductor or U- or I- shaped shields

which are located between the conductors. Although these shields are connected to the ground plane, they are not used as wiring lines.

As in this document only a single wiring layer is present, the problem of cross-talk between signal lines of different wiring layers is not addressed.

3.6 The examining division argued in the contested decision, that the skilled person, aware of the underlying physical principles of electromagnetically shielding conductive structures, would have provided some kind of shield along an imaginary line interconnecting the wiring lines to be shielded, independently of the fact that these wiring lines are located in the same or different wiring planes.

However, claim 1 of the application in suit is not directed to a basic physical principle of electromagnetic shielding, but relates to a solution, albeit based on the principle, to the problem of cross-talk between signal lines in different wiring planes. Documents D1 and D4 do not address this problem, but only address the problem of cross-talk between coplanar signal lines.

Although document D4 discloses a wall-like shielding structure, this is to provide shielding between co-planar signal lines. Also, such a wall structure would not be compatible with the orthogonal arrangement of the wiring lines belonging to different wiring layers disclosed in document D1.

3.7 For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive

step in the sense of Article 56 EPC and accordingly meets the requirements of Article 52(1) EPC.

Dependent claims 2 to 6 concern further particular embodiments of the invention and are patentable for the same reasons.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents as specified under item V above.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla