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D E C I S I O N
of 7 December 2001

Case Number: T 0923/96 - 3.4.3

Application Number: 89304006.3

Publication Number: 0365107

IPC: H01L 21/331

Language of the proceedings: EN

Title of invention:

Manufacturing method for vertically conductive semiconductor devices

Applicant:

KABUSHIKI KAISHA TOSHIBA

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step (no)"

Decisions cited:

-

Catchword:

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Boards of Appeal

Chambres de recours

Case Number: T 0923/96 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 7 December 2001

Appellant:

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Decision under appeal:

**Decision of the Examining Division of the
European Patent Office posted 24 May 1996
refusing European patent application
No. 89 304 006.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
M. J. Vogel

Summary of Facts and Submissions

I. This is an appeal from the decision of the examining division, dispatched 24 May 1996, to refuse European patent application No. 89 304 006.3 on the ground that the invention as claimed in claim 1 did not involve an inventive step in view of the following prior art document:

D1: EP-A-0 192 229

II. The notice of appeal was filed on 24 July 1996 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was furnished on 23 September 1996.

III. In response to a written communication in which the Board indicated, *inter alia*, that the invention as claimed appeared to be obvious, the appellant filed on 7 November 2001 a new set of claims as main request, and two further sets of claims as first and second auxiliary requests, respectively. Claim 1 of the main request reads as follows:

"1. A method for manufacturing a vertical conducting power semiconductor device having a cathode, an anode and a gate electrode, comprising the steps of:

preparing a highly doped semiconductor substrate (1) of a first conductivity type;

forming a first semiconductor layer (2) on said semiconductor substrate which has a lower impurity concentration than that of said semiconductor substrate (1);

forming a highly doped second semiconductor layer (3) of a second conductivity type on said first semiconductor layer (2);

forming a lightly doped third semiconductor layer (4) of said second conductivity type on said second semiconductor layer (3); and

forming a first impurity doped region (6) of said first conductivity type in said third semiconductor layer which is diffused from a surface of said third semiconductor layer by a heating process,

characterised by diffusing impurities of first conductivity type of said semiconductor substrate into said first semiconductor layer (2) and causing said first semiconductor layer (2) to disappear when said impurity doped region is diffused by said heating process, so as to maintain the impurity concentration of said second semiconductor layer at a constant level and substantially maintain the same thickness."

Claim 1 of the first auxiliary request differs from claim 1 of the main request by the addition at the end of the claim of the statement "wherein said first, second and third layers are formed by an epitaxial growth technique."

Claim 1 of the second auxiliary request differs from claim 1 of the main request by the addition at the end of the claim of the statement "the thickness of said second semiconductor layer being within the range from 5 μm to 10 μm ."

IV. Oral proceedings took place on 7 December 2001.

- V. The arguments submitted by the appellant in support of his requests can be summarised as follows.

The main request

The nearest prior art document D1 relates in general to the problem of preventing the effects of diffusion during processing. The major difference in relation to the method of the present invention is that the manufacture of the device in document D1 involves the joining of two separate substrates. The main barrier against diffusion would appear to be the interface between the two joined substrates on account of the boundary layer which is formed between the two semiconductor substrates and which is crystallographically different from those substrates.

As stated in the introduction to the description, the invention of the application in suit aims to provide a device which combines fast switching speed with a low ON resistance. It is accepted as known that a thin high impurity concentration n+ buffer layer provides both high speed switching and a low ON resistance.

If the n+ buffer layer is formed on a p+ substrate as is customary for such devices, diffusion from the p+ substrate during subsequent processing will cause the n+ layer to be modified in both doping concentration and thickness. The invention as claimed therefore proposes that an intermediate layer, the first semiconductor layer 2 of claim 1, be provided between the semiconductor substrate and the buffer layer, with

the intermediate layer being such that it disappears when subsequent diffusion processes used to form further device structures have been completed.

Although the p- type silicon layer 50 shown in Figure 5 of document D1 admittedly has the effect of preventing diffusion from the p+ substrate into the n+ layer-like region 32, the skilled person would, for the following reasons, not have considered modifying the process described in document D1 in such a way as to make the p- layer 50 disappear at the end of the diffusion processing.

The process described in Document D1 provides a cheap method of forming vertically conducting high power semiconductors. The crystal quality at the junction between p and n+ is clearly not considered important in document D1. Since the manufacturing process for making the devices as described in document D1 is difficult to control, a graded p-n junction is, in fact, advantageous so that the skilled person would be induced to retain the p-type silicon layer 50. In contrast, in the case of the invention in suit, the junction is grown since a high quality junction is aimed for in order to achieve the desired high switching speed and low ON resistance. Only with the benefit of hindsight would the skilled person have considered modifying the process described in document D1 such that on completion of the device the intermediate p- layer 50 would have disappeared. The invention as claimed in claim 1 of the main request is therefore not obvious over the disclosure in document D1.

First auxiliary request

Compared to claim 1 of the main request, claim 1 of the first auxiliary request further specifies that the junction is an epitaxially grown junction. This further distinguishes the claimed invention from the disclosure in document D1. Moreover, document D1 teaches away from epitaxially growing the n+ layer on the p+ substrate. The first auxiliary request is therefore clearly distinguished from the teaching of the prior art document D1. It should also be born in mind that at the priority date of the application in suit it was not at all clear in which technical direction the solution to obtaining improved devices was going to be found. Thus, for example, US patent 4 696 701 cited in the search report but not during examination, which was published just before the priority date of the application in suit, provides for a highly doped "sealing layer" which becomes a passive part of the final device structure. This document demonstrates that, there was no prejudice against having a highly doped layer included in the final device structure. If therefore supports the view that, at the priority date of the application, there was no motivation to modify the device of document D1 in a way which makes the intermediate layer disappear.

Second auxiliary request

Claim 1 of the second auxiliary request differs from claim 1 of the main request in that it defines the width of the n+ buffer layer. The technical problem and its solutions are therefore as in the main request, but the claim is restricted to a 5 to 10 μm thick buffer layer.

In contrast in document D1 the buffer layer is approximately 15 μm thick. The quoted dimensions for

the n+ type buffer layer of document D1 of between 5 to 30 μm are considered to be a misprint and should have read "between 25 and 30 μm " as in the original Japanese publication from which priority is claimed.

Reasons for the Decision

1. The appeal is admissible.
2. *Inventive step (Articles 52(1) and 56 EPC)*

The main request

- 2.1 Document D1, the nearest prior art, concerns the manufacture of vertically conducting high power semiconductor devices. In the words of claim 1 of the main request, document D1, with particular reference to Figure 5, discloses a method for manufacturing a vertical conducting power semiconductor device having a cathode, an anode and a gate electrode, comprising the steps of:

- (i) preparing a highly doped semiconductor substrate (30) of a first conductivity type (p+); forming a first semiconductor layer (50) on said semiconductor substrate which has a lower impurity concentration (p-) than that of said semiconductor substrate (50);
- (ii) forming a highly doped second semiconductor layer 32 of a second conductivity type (n+) on said first semiconductor layer 50;
- (iii) forming a lightly doped third semiconductor

layer (31) of said second conductivity type (-) on said second semiconductor layer (32); and

- (iv) forming a first impurity doped region 37 of said first conductivity type in said third semiconductor layer which is diffused from a surface of said third semiconductor layer by a heating process; characterised by diffusing impurities of first conductivity type of said semiconductor substrate into said first semiconductor layer (50).

2.2 The only distinguishing feature of the invention as claimed in claim 1 of the main request is therefore that the first semiconductor layer is caused to disappear when the impurity doped region is diffused by said heating process, as a result of which the impurity concentration of the second semiconductor layer is maintained at a constant level and substantially the same thickness.

2.3 It had already been remarked by the examining division that the reason for providing the layer 50 in document D1 is the same as the reason for providing the intermediate layer 3 in the invention as claimed, that reason being to protect the highly doped n+ buffer layer against diffusion from the highly doped p+ substrate.

2.4 The appellant has argued that document D1 teaches away from the invention in that in document D1 a graded junction is preferable for manufacturing purposes, since in a less well controlled manufacturing process a graded junction provides more predictable device performance. However, the Board takes the view that the

skilled person would have been well aware that a graded junction, and the presence of a lightly doped layer in the vicinity of the junction as in document D1 would reduce the switching speed and increase the ON-resistance and that, in order to aim for an improved device with lower ON-resistance and higher switching speed, the presence of the lightly doped layer 31 was undesirable. The skilled person therefore has an incentive to consider modifying the process described in document D1 by removing the lightly doped layer.

- 2.5 Determining diffusion of a dopant in a given time at a given temperature is well within the range of skills required of the person skilled in the art as demonstrated, for example, by the fact that the same skilled person is required to determine the diffusion parameters for the formation of the diffused region 37 of Figure 5 of document D1 and of the diffused regions 6, 10, 101 and 25 of Figure 4(a) to (g) and 7(a) to (c) of the application in suit. Making the lightly doped layer disappear in order to improve the device performance with respect to switching speed and ON resistance, while at the same time protecting the n+ layer against the effects of out diffusion from the heavily doped substrate is therefore to the person skilled in the art of semiconductor device manufacture merely a matter of optimising the thickness and doping level of the lightly doped layer such that the out diffusion from the heavily doped substrate extends through but not beyond the lightly doped layer in the time it takes to form other diffused device regions.

- 2.6 The beneficial effect of an n+ type thin layer in a vertically conducting semiconductor device is explained on page 3 line 26 to page 4 line 5 of document D1,

which further states that if an n+ type thin layer region is properly controlled in impurity concentration and in thickness, "an increase of the ON resistance can be set within a negligibly range and at the same time the turn off time can be reduced to a greater extent". There is, therefore also an incentive to maintain the n+ layer at the same thickness and impurity concentration throughout the subsequent processing.

First auxiliary request

2.7 Claim 1 of the first auxiliary request differs from claim 1 of the main request in that it additionally specifies that the junction is epitaxially grown. The appellant has submitted that this restriction to epitaxially grown junction provides a further important distinction over the prior art as described in document D1, since document D1 explicitly teaches away from using epitaxial growth to form the n+ buffer layer and n- type drain region (page 4 lines 30 to 34, "it is very difficult to form the n+ type layer-like region and n- type drain region... by the vapour growth method on the p+ type semiconductor layer...without forming the inversion layer").

2.8 The Board is not persuaded by this argument. While document D1 admittedly states that it is very difficult to form by chemically vapour position the n+/n layer structure on top of the p+ semiconductor layer, this admission of difficulty is not the same as creating a technical prejudice against epitaxial growth as such. Moreover the invention disclosed in document D1 purports to a marked decrease in the difficulty of **mass production** in comparison with the vapour growth method, thereby assuring lower cost due to mass production

(page 10 lines 14 to 17).

- 2.9 Document D1 thus discloses both the method of joining substrates to form devices as well as forming devices by epitaxial growth, with the advantages of the joining method being perceived to lie in providing mass produced devices reliably and cheaply. However, the document does not teach away from the well known advantage of obtaining better quality devices through epitaxial growth. In addition, the protection of the n+ layer against out-diffusion from the substrate by means of the lightly doped p layer formed on top of the heavily doped substrate is applicable whatever the manufacturing method employed. The Board therefore concludes that additionally specifying that the layers are formed epitaxially does not confer a patentable distinction on the claim.

Second auxiliary request

- 2.10 Claim 1 of the second auxiliary request has the same wording as claim 1 of the main request with the additional feature that the width of the n+ buffer layer is defined as lying between 5 and 10 μm .
- 2.11 Document D1 describes that the n+ buffer layer is initially formed at the thickness of 5 to 30 μm (page 9 line 34 to page 10 line 2). The appellant has argued that the lower limit of 5 μm appears to be a typographical error and that the thickness range for the n+ type silicon layer should read 15 to 30 μm or even 25 to 30 μm , in view of the inversion layer being referred to as being usually about 10 μm in thickness.

While the thickness of the n+ layer will have an

influence on the thickness of the inversion layer formed in the n- region beyond the n+ layer, there is no compelling reason for assuming that the character of the inversion layer would be changed in any way if the n+ silicon layer is of a thickness of greater than 5 µm. Moreover the subsequent paragraph (page 10 lines 3 to 6) clearly states that the "inversion phenomenon can be suppressed due to the presence of the p-layers, so that control of the highly doped buffer layer is made easier." The Board does not therefore consider that the particular range of thickness for the buffer layer chosen in claim 1 of the auxiliary request shows any indication of involving an inventive step.

3. In the Board's judgement, therefore, the invention as claimed in claim 1 of each of the main request and the first and second auxiliary request does not involving an inventive step as required by Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla