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**D E C I S I O N**  
**of 23 August 2000**

**Case Number:** T 0874/96 - 3.4.3

**Application Number:** 90113757.0

**Publication Number:** 0418491

**IPC:** H01L 27/108

**Language of the proceedings:** EN

**Title of invention:**

DRAM cell with trench capacitor and buried lateral contact

**Applicant:**

TEXAS INSTRUMENTS INCORPORATED

**Opponent:**

-

**Headword:**

DRAM cell with a trench capacitor/TEXAS INSTRUMENTS

**Relevant legal provisions:**

EPC Art. 123(2), 56

**Keyword:**

"Inventive step - yes"  
"Amendments - allowable"

**Decisions cited:**

-

**Catchword:**

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Case Number: T 0874/96 - 3.4.3

**D E C I S I O N**  
of the Technical Board of Appeal 3.4.3  
of 23 August 2000

**Appellant:** TEXAS INSTRUMENTS INCORPORATED  
13500 North Central Expressway  
Dallas  
Texas 75265 (US)

**Representative:** Leiser, Gottfried, Dipl.-Ing.  
Prinz & Partner GbR  
Manzingerweg 7  
D-81241 München (DE)

**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 25 April 1996  
refusing European patent application  
No. 90 113 757.0 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** E. Wolff  
W. Moser

## Summary of Facts and Submissions

- I. European patent application No. 90 113 757.0 was refused in a decision of the examining division, dated 25 April 1996 on the ground that the application as amended did not comply with Article 123(2) EPC. In particular, amended claim 1 specifying that the second insulating material has an etch rate substantially different from that of the material of the first insulating layer was found to lack any basis in the claims and in the description of the relevant embodiment of Figures 10 H and 10 I of the application as filed. Also, in the decision under appeal, essential features of the invention were identified and it was observed that a new main claim containing these features would meet the requirements of Article 84, Article 123(2), and Article 52(1) of the EPC (cf. points 3.1, 3.2 and 3.4 of the reasons).
- II. The appellant filed a notice of appeal against the above decision on 28 June 1996 and paid the appeal fee on the same date. The statement of the grounds of appeal along with new claims and new pages of the description forming the basis of a main request and an auxiliary request were filed on 29 August 1996. The appellant also requested oral proceedings in the event that the Board intended to dismiss the appeal.
- III. In an annex to the summons to the oral proceedings, the Board took the view that claims 1 of the main request and the auxiliary request, respectively, were not clear and that claim 1 of the main request did not comply with Article 123(2) EPC.

In response, the appellant filed a new claim 1 of a

main request and new claims 1 to 4 of an auxiliary request on 24 July 2000.

- IV. At the oral proceedings held on 23 August 2000, the appellant submitted a main request and an auxiliary request, the main request being as follows:

To set aside the decision under appeal and to grant a patent on the basis of the following documents:

**Claims:** 1 as submitted during the oral proceedings as the main request, and 2 to 7 as filed on 12 May 1995

**Description:** pages 1 to 3, 3a, 4 to 10 as filed on 29 August 1996; and

**Drawings:** Sheets 1/11 to 11/11 as filed on 11 January 1994.

- V. The sole independent Claim 1 according to the main request has the following wording:

"A process for forming a DRAM cell, comprising the steps of:

forming a trench (218, 200) in a substrate (210);  
forming a first insulating layer (222) comprising a first insulating material on a surface of the trench ;  
forming a first conductive layer (228) on said first insulating layer;  
forming a second insulating layer (232) on the first conductive layer, the second insulating layer comprising a second insulating material;  
forming a second conductive layer (238) on said second

insulating layer so as to complete a capacitor (213);  
removing by selective etching in relation to the first  
conductive layer a portion of said first insulating  
layer between the surface of the trench and the first  
conductive layer to provide a cavity (240) extending  
into said trench;  
filling said cavity with a conductive material (242,  
246);  
forming a field effect transistor (211) on the  
substrate adjacent to the trench, one source/drain  
(268) of the transistor being conductively connected to  
said conductive material."

Claims 2 to 7 are dependent on claim 1.

VI. The submissions made by the appellant in support of his  
main request can be summarised as follows:

In the decision under appeal, claim 1 as amended was  
considered to meet the requirements of the Convention,  
in particular of inventive step. Moreover, as submitted  
by the appellant in its response dated 10 January 1994  
during the examination proceedings, document D1  
(EP-A-0 264 858 ) discloses a capacitor structure  
formed in a trench and a sidewall contact on the  
surface of the substrate to provide electrical contact  
between a capacitor plate and the associated  
transistor. There is no teaching in the document of a  
lateral contact extending below the substrate surface.

In the method described in document D2 (PATENT ABSTRACT  
OF JAPAN, vol. 13, no. 468 (E-468) [3816, 23 October  
1989; & JP-A-1 183 152), an etching mask is required in  
etching a portion of a capacitor dielectric layer with  
a view to providing a lateral contact below the

substrate surface. This method would not be applicable on the structure disclosed in document D1 since it would not be possible to mask the structure to expose only the first insulating layer which is to be etched. Moreover, the structure in document D1 has a silicon dioxide region 28 with lateral regions 28a extending beyond the trench walls so as to prevent the etching of a conformal layer 30. These lateral regions would also prevent etching of the first insulating layer 26 to produce a subsurface lateral contact using the method of document D2.

The subject-matter of claim 1 is thus not a straightforward design option moving from the DRAM cell of document D1 to the DRAM cell of the present invention, and is inventive over documents D1 and D2.

### **Reasons for the Decision**

1. The appeal complies with the requirements of Articles 106 to 108 and Rule 64 EPC and is therefore admissible.
  
2. *Amendments - Main request*

Claim 1 has been amended in relation to claim 1 forming the basis of the decision under appeal inter alia in that the statement to the effect that the second insulating material has a substantially different etching rate than the first insulating layer has been deleted from the latter claim. Thus, the subject-matter which was considered in the decision under appeal to go beyond the content of the application as filed, and therefore to contravene Article 123(2) EPC, does not

form part of the claimed subject-matter.

Claim 1 has been amended in relation to claim 1 as filed in that

- (i) the amended claim requires that a portion of the first insulating layer is removed by **selective etching in relation to a first conductive layer** and
- (ii) it is made clear in the claim that the portion of the first insulating layer which is removed is between **the surface of the trench** and the first conductive layer.

In the application as filed, a process for forming a DRAM cell according to the invention as claimed is described with reference to Figures 10A to 10Q. After the formation of a structure as shown in Figure 10H, the structure is subjected to an isotropic silicon dioxide etch, whereby the top portion of the silicon dioxide layer 221 provided on a surface of the trench wall is removed and an opening, i.e. a cavity between the surface of the trench wall and the first conductive layer 232 is formed (cf. page 18, lines 4 to 10). It is clear from this process step that during the etching both the silicon dioxide layer 221 and the conductive layer are exposed to the etchant, and only a portion of the silicon dioxide layer is removed by etching, i.e. the silicon dioxide is etched selectively in relation to the first conductive layer.

Thus, the above amendments (i) and (ii) are disclosed in the application as filed, so that the claim as amended does not go beyond the content of the

application as filed and meets the requirement of Article 123(2)EPC.

The description and the drawings of the application as filed have been amended for consistency with the amended claims and therefore comply with Article 123(2) EPC as well.

3. *Inventive step*

3.1 As stated in item I above, in the decision under appeal, an independent claim containing the features as in claim 1 of the main request and additionally specifying that the first and second insulating layers are of different insulating materials was considered to meet the requirements of the Convention including that of inventive step.

In the Board's view, however, the subject-matter of claim 1 involves an inventive step notwithstanding the fact that the claim does not specify that the materials of the first and the second insulating layers are different, for the following reasons:

3.1.1 Document D1 describes a process for forming a DRAM cell having a trench capacitor, comprising a first insulating layer 26 on the surface of a trench wall, a first conductive layer 22 on the first insulating layer, a second insulating layer 26A on the first conductive layer and a second conductive layer 24 filling the trench. The first and second conductive layers form the capacitor electrodes and the second insulating layer acts as the capacitor dielectric, as in the present invention. The process described in document D1 is however concerned with forming a



capacitor having a mandrel structure which protrudes above the trench, i.e the surface of the substrate, and a self-aligned bridge contact 30 having a horizontal surface and a vertical surface on the sidewall of the mandrel to connect the first conductive layer 22 electrically to a region 36 of a transistor (cf. in particular, column 10, lines 3 to 6, lines 14 to 16; column 11, lines 49 to 53 and column 11, line 56 to column 12, line 2; column 13, lines 17 to 56; and Figures 5 to 9A). In the formation of the self-aligned bridge contact, an oxidation pattern 28 having lateral ends 28A that overhang the sidewalls of trench 20 is formed on the capacitor structure. The lateral ends act as an etching mask in the formation of the bridge contact by etching of a polysilicon layer 30A (cf. Figure 9A ).

The process according to claim 1 of the application in suit, on the other hand, is concerned with the formation of a DRAM cell having a capacitor which is located within a trench and the formation of an electrical contact between the capacitor and a field effect transistor of the cell. The electrical contact according to the claimed process is formed by removing by selective etching a portion of a first insulating layer provided on the surface of the trench so as to form a cavity extending into the trench and then filling the cavity with a conductive material, whereby the surface area occupied by the cell is minimized.

Document D2 teaches to form an electrical contact 28 between a trench capacitor and a source/drain region 31 of a field effect transistor by filling a cavity with a conductive material located on the upper end of the inner face of the trench (see the abstract). To this

end, as can be seen from Figure 5(d), the dielectric layer 27 of the capacitor is removed by using a mask 41. In the process according to the claimed invention on the other hand, the cavity is formed by etching the first insulating layer which isolates the capacitor structure from the trench and not by etching the capacitor dielectric. Thus, a direct application of the teaching of document D2 regarding the etching of the dielectric layer 27 would not result in the removal of the first insulating layer as in the claimed invention.

Moreover, the processes in documents D1 and D2, respectively, are directed to producing completely different capacitor structures. Thus, whereas the capacitor in document D1 is isolated from the trench by an insulating layer and has a mandrel structure with a sidewall contact, in document D2 the substrate itself forms one electrode of the capacitor which is entirely located in a trench, and the electrical contact extends in the trench. Therefore, a skilled person concerned with the formation of a DRAM cell, as in the present invention, would not arrive at the claimed process without substantially modifying the processes respectively of the documents D1 and D2. Thus, for example, in document D1, all the process steps leading to the formation of the mandrel structure and the formation of the self-aligned sidewall contact would need to be abandoned, which raises serious doubts as to whether the process in D1 can be regarded as relevant to the formation of a DRAM cell as in the present invention. Also, the modifications necessary to arrive at the claimed invention, are not suggested in the cited documents and, in the Board's judgement, cannot therefore be regarded as obvious within the meaning of Article 56 EPC.

For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC and meets the requirements of Article 52(1) EPC.

## Order

### For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent on the basis of the following documents:

**Claims:** 1 submitted during the oral proceedings as main request, and 2 to 7, filed on 12 May 1995;

**Description:** pages 1 to 3, 3a, 4 to 10, filed on 29 August 1996; and

**Drawings:** sheets 1/11 to 11/11, filed on 11 January 1994.

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla