BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen
(D) [ ] No distribution

D E C I S I O N
of 12 March 2002

Case Number: T 0636/96 - 3.4.3

Application Number: 90307846.7

Publication Number: 0410633

IPC: H01L 21/76

Language of the proceedings: EN

Title of invention:
Planar isolation technique for integrated circuits

Applicant:
AT&T Corp.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 52, 54, 56, 84

Keyword:
"Clarity (yes - after amendments)"
"Novelty (yes - after amendments)"
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0636/96 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 12 March 2002

Appellant: AT&T Corp.
32 Avenue of the Americas
New York, NY 10013-2412 (US)

Representative: Williams, David John
Page White & Farrer
54 Doughty Street
London WC1N 2LS (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 21 February 1996 refusing European patent application No. 90 307 846.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
J. Van Moer

Summary of Facts and Submissions

I. European patent application No. 90 307 846.7 was refused by the decision of the examining division dated 21 February 1996. The ground for the refusal was that the subject-matter of independent claim 17 of the set of claims 1 to 19 according to the applicant's request dated 20 July 1995 was not new (Article 54 EPC) having regard to the prior art document

D1: EP-A-0 220 392

In the decision under appeal the examining division further observed that independent claim 1 of the above request was not clear (Article 84) and that the subject-matter of independent claims 1 and 11 extended beyond the content of the application as filed (Article 123(2) EPC). Claims 1 and 11 were, for these reasons, not admissible. Also, according to the decision, the subject-matter of claim 1, even when amended to comply with Articles 84 and 123(2) EPC, would not be new having regard to the disclosure of document D1.

II. Independent claim 1 of the above request reads as follows:

"1. A semiconductor device comprising (1) a substrate, (2) first and second active regions and (3) a region of dielectric material, said dielectric material positioned within said device and having a geometric shape to limit interaction of charge or electric field through said substrate

characterized in that

said dielectric material occupies a trench between said first and second active regions

and an electrically conductive region is present in said dielectric material along the sidewalls of said trench adjacent said active regions

wherein said conductive region is less than about 200 nm in thickness measured along the direction perpendicular to said sidewall at the midpoint between the lowest point of said trench and the upper major surface of said substrate

and said conductive region is separated from said active region by a portion of said dielectric material

and wherein said conductive region is maintained at essentially the same potential as said substrate."

Claims 2 to 10 and 12 to 16 of the above request related to a semiconductor device and were dependent on claims 1 and 11, respectively. Independent claims 17, 18 and 19 of the request related to a process for fabricating a semiconductor device.

III. The appellant (applicant) lodged an appeal on 18 April 1996. The appeal fee was paid on the same date. The statement setting out the grounds of appeal was filed on 24 June 1996.

IV. In response to communications from the Board, the appellant submitted with his letters dated 16 July 2001 and 23 January 2002 amended claims and description pages and requested that the decision under appeal be set aside and a patent be granted on the basis of the

following documents:

Claims: 1 to 6 filed with the letter dated 23 January 2002
7 and 8 filed with the letter dated 16 July 2001

Description: pages 1, 6 and 9 as originally filed
page 8 as filed with letter dated 16 July 2001
pages 2, 2a, 3 to 5 and 7 as filed with letter dated 23 January 2002

Drawings: Sheets 1/3 to 3/3 as originally filed

V. The wording of the independent claim according to this request is as follows (subdivided into paragraphs (a) to (f) by the Board for facilitating discussion):

"1. A semiconductor device comprising (1) a substrate, (2) first and second active regions and (3) a region of dielectric material,

(a) said dielectric material (34, 35) positioned within said device to limit interaction of charge or electric field through said substrate,

(b) wherein said dielectric material (34, 35) occupies a trench between said first and second active regions,

(c) wherein an electrically conductive region (30) is present in said dielectric material (34, 35) along the sidewalls of said trench adjacent said active regions,

(d) wherein said conductive (30) region is between

about 20 and 200 nm in thickness measured along the direction perpendicular to said sidewall at the midpoint between the lowest point of said trench and the upper major surface of said substrate,

(e) and wherein said conductive region (30) is separated from said active region by a portion (35) of said dielectric material, characterized in that

(f) the conductive region (30) is in electrical contact with the substrate via a connecting region (37), such that the conductive region (30) is held at essentially the same potential as the substrate."

Claims 2 to 8 are dependent claims and relate to a semiconductor device.

VI. The appellant has argued essentially as follows:

- The object of the invention is to provide isolation between adjacent device regions in a substrate while providing a planar surface for device fabrication and avoiding excessive capacitance due to this isolation. This is achieved by a dielectric filled trench structure having a conductive region within the dielectric material, wherein the conductive region is located along the sidewalls of the trench and is maintained at the same potential as the substrate.

- Document D1 does not disclose a grounded conductor within a trench structure located at the position of runners crossing the field oxide. The semiconductor device according to the invention is therefore new over this disclosure.

- Moreover, as document D1 relates to a method of making trench capacitors, its teaching is directed to enhance and not to decrease the capacitance of the obtained structures and points away from the present invention.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments (Articles 84 and 123(2) EPC)

2.1 The examining division observed in the decision under appeal that the expression "said dielectric material positioned within said device and having a geometric shape to limit interaction of charge or electric field through said substrate" used in claim 1 was unclear, since the reference to a particular geometric shape was an attempt to define the claimed device in terms of the result to be achieved. However, no reference to a particular geometric shape to achieve the specified effect could be found in the originally filed application documents.

This expression has been replaced, according to the appellant's request, by "said dielectric material positioned within said device to limit interaction of charge or electric field through said substrate". It overcomes the clarity objection raised by the examining division, since a particular geometric shape of the trench is no longer specified as being a requirement for achieving the specified effect. As the examining division correctly pointed out, no such requirement is derivable from the description and, in the Board's

view, any dielectric filled trench positioned within a substrate limits the interaction of charge or electric field through said substrate.

2.2 Present claim 1 further differs form claim 1 as filed by the addition of paragraphs (d) to (f) (cf. point VI). These amendments are disclosed in column 3, lines 34 to 39; column 3, lines 31 to 33 and column 4, lines 17 to 20 of the published application, respectively.

2.3 The application as amended complies therefore with Articles 84 and 123(2) EPC.

2.4 The objections raised by the Examining Division in respect of claims 11 and 17 are no longer valid, as these claims and the corresponding embodiments have been deleted from the application.

3. Novelty (Article 54 EPC)

3.1 Document D1 discloses a capacitor structure formed on the sidewalls of mesa-shaped silicon regions. Active or passive devices are located on the mesa-shaped silicon regions and the mesas are separated from each other by trenches 19. The dielectric filled trenches isolate the devices formed on adjacent mesas and limit their mutual electric interaction. A capacitor is formed on the sidewalls of the mesa structure as follows: the mesa's silicon material 12 serves as the first plate of the capacitor, a thin dielectric layer 21 formed on the vertical sidewalls of the mesa serves as the capacitor's insulator and a thin conductive polysilicon layer 22 formed directly over the capacitor's insulator serves as the second plate of the capacitor. The

remaining part of the trench is filled with a dielectric material (cf. Figures 1 to 4; column 4, line 39 to column 5, line 5; column 7, lines 28 to 31 and column 7, line 55 to column 8, line 31).

According to this document, the conductive polysilicon layer 22 has an initial thickness of about 200 to 300 nm. After having been formed, it is oxidized to form a thin silicon dioxide layer 23 of a thickness of about 50 to 100 nm (cf. column 8, lines 3 to 18). As the thickness of the polysilicon layer is reduced due to this oxidation process, it is the Board's view, that the final thickness of the polysilicon layer 22 falls within the range of 20 to 200 nm specified in paragraph (d) of claim 1.

In summary, document D1 discloses a semiconductor device having the features specified in paragraphs (a) to (e) of claim 1 (cf. point VI).

3.2 However, an electrical interconnection between the polysilicon layer and the silicon substrate, ie the features of paragraph (f) of claim 1, is not disclosed in this document.

In consequence, the semiconductor device according to claim 1 of the application in suit is new.

4. Inventive step (Article 56 EPC)

4.1 The semiconductor device according to claim 1 and the capacitor structure disclosed in document D1 differ by the features of paragraph (f).

4.2 The Board concurs with the applicant that it is an

object of the invention to provide isolation between adjacent device regions while providing a planar surface for device fabrication and avoiding excessive capacitance due to this isolation. A planar device surface is required for high lithographic resolution and accurate etching. However, thinning the dielectric region to limit the non-planarities has the drawback that the electric field produced by the runners crossing the dielectric may influence the underlying semiconductor substrate. Due to this interaction the device speed is reduced, since thinning the dielectric increases the capacitance of the runners. Furthermore, the electric field of the runners may generate an inverted region in the silicon substrate degrading therefore the performance of the active regions due to leakage currents between these regions (cf. the published application, column 1, line 44 to column 2, line 30).

The provision of a grounded conductive region within the trench permits the reduction of the thickness of the dielectric region, improving thus the planarity of the device, without increasing the electric interaction between the runners and the semiconductor substrate.

In consequence, in the Board's view, the electrical connection between the conductive region and the substrate solves the problem stated in the application in suit.

4.3 Document D1 concerns the provision of a high capacitance integrated trench capacitor structure without increasing the device's size (cf. D1, column 1, lines 4 to 7). In spite of the structural similarities between the capacitor structure disclosed in this

document and the isolation trench structure of the application in suit, no technical link exists between these structures as they serve two different purposes.

In particular, a skilled person would not consider to provide an electrical connection between the plates of the capacitor, ie between the semiconductor substrate 12 and the conductive polysilicon layer 22, disclosed in document D1, since all capacitive effect would then be lost.

For these reasons, it is the Board's view that a skilled person would not have considered the capacitor structure disclosed in document D1 to solve the problem addressed in the application in suit.

5. In the Board's judgement, therefore, the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC and meets the requirements of Article 52(1) EPC.

Dependent claims 2 to 8 concern further particular embodiments of the invention which are patentable for the same reasons.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent with the

documents mentioned under point IV. above.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla