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D E C I S I O N
of 12 March 1998

Case Number: T 0149/96 - 3.5.2

Application Number: 92201468.3

Publication Number: 0516230

IPC: H03K 3/037

Language of the proceedings: EN

Title of invention:
Electronic flip-flop circuit, and integrated circuit comprising the flip-flop circuit

Applicant:
Philips Electronics N.V.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54(2), 84, 96(2), 113(1), 123(2)
EPC R. 51(2),(3), 67

Keyword:
"Procedural violation"
"Remittal to the first instance"
"Reimbursement of the appeal fee"
"Copy of cited prior art sent to applicant deviated from published form"

Decisions cited:
T 0161/82, T 0162/82, T 0042/84

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0149/96 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 12 March 1998

Appellant: Philips Electronics N.V.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 19 September 1995 refusing European patent application No. 92 201 468.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: A. G. Hagenbucher
A. C. G. Lindqvist

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 92 201 468.3. The reason given for the refusal was that the subject-matter of claim 1 as originally filed was not novel, having regard to the following prior art document:

D1: EP-A-219 846.

II. Claim 1 as originally filed is worded as follows:

"1. An electronic flip-flop circuit having a data input, a data output and a clock signal input, and comprising a first transfer gate for transferring, under the control of the clock signal, data from the data input to an input of a first storage element, and a second transfer gate for transferring, under the control of the clock signal, data from an output of the first storage element to an input of a second storage element, an output of which constitutes the data output, the transfer gates being directly driven by the same clock signal, characterized in that the second transfer gate comprises means for prolonging the transfer time for data from the first to the second storage element."

III. In the first and only communication pursuant to Article 96(2) and Rule 51(2) EPC dated 11 April 1995 a number of correspondences between the subject-matter of the above cited claim 1 and the flip-flop disclosed in document D1, Figure 8 in conjunction with Figures 6(a) and 6(b) and claim 1, in particular data input, data output, clock signal input, first transfer gate, first

storage element, second storage element and second transfer gate, were pointed out. It was concluded therefrom that the subject-matter of claim 1 was not novel and the claim not allowable. In further paragraphs of the communication the only embodiment disclosed in the present application (shown in Figure 4) was analysed. Attention was drawn to differences between this embodiment and the prior art known from D1. The meaning of the term "transfer gate" was discussed. The communication hinted at the possibility of drafting a new independent claim including the features shown in Figure 4 of the present application, and that the preamble of such a new claim should be based on D1.

IV. In the reply dated 28 July 1995 to this communication the applicant (now appellant) observed that the feature "the transfer gates being directly driven by the same clock signal" in claim 1 was not among the correspondences pointed out in the communication and was not taught by document D1. According to Figure 8 of D1 the transfer gates were controlled by signals of opposite phase. Therefore the subject-matter of claim 1 as filed was novel over D1. No other ground for rejecting the application had been raised. The applicant offered to insert a definition of the term "transfer gate" into the description, but maintained the claims unamended.

V. In the decision under appeal the examining division referred to the correspondences between the subject-matter of claim 1 and that of D1 set out in the communication and agreed that the feature "the transfer gates being directly driven by the same clock signal" had not been dealt with in the communication expressis verbis. The examining division reasoned, however, that among the indicated correspondences "there was a reference to first and second transfer gates (which,

and this goes without saying, own a respective control input) and to a clock signal input (clock signal phi). Hence, it was implicit in the statements provided in said communication - and therefore evident to any reader of the communication - that also the connection between the clock signal input and the (control inputs of) the transfer gates was meant to be the same as that understandable from present claim 1.". Furthermore, the phrase "the transfer gates being directly driven by the same clock signal" could readily be read onto the D1 reference. Both transfer gates G1 and G3 in Figure 8 in D1 were actually driven by the same clock signal (phi), regardless of whether the gates were responsive to different phases of said signal. The relevant (single) clock signal was represented by signal phi. This view was corroborated by the wording of claim 1 in D1: namely "controlling said master latch circuit (M) by a control signal (phi)" in column 6, lines 24 and 25, and "controlling said slave latch circuit (S) by said control signal (phi)" in column 6, lines 40 and 41. In the opinion of the examining division the suggested insertion of the definition of the term "transfer gate" appeared to contravene Article 123(2) EPC. In spite of the examining division's suggestion for amending claim 1, the appellant maintained the application with the original claims.

VI. In support of the appeal the appellant essentially argued that the decision under appeal had been based on grounds on which the appellant had not been able to comment beforehand. In the decision under appeal the examining division had for the first time attached to the words "clock signal" the meaning of an abstract signal which could be said to control different transfer gates even when two complementary voltages

were needed. This was also the meaning D1 gave to the words "clock signal" in its claim 1. There was, however, no basis for giving this abstract meaning to the words "clock signal" in the present application, nor was this abstract meaning the normal meaning of these words. The present application emphasised the use of a single clock signal rather than complementary versions of the abstract clock signal. To the extent that the rejection for lack of novelty was based on such an interpretation it was therefore unfounded. In the decision under appeal the examining division argued that it had **implicitly** stated that the clock signal connection to the transfer gates in Figure 8 of D1 was such as indicated in claim 1, i.e. directly driven by the same signal. The appellant was expected to understand this from the fact that a novelty objection was raised, even though this feature was not mentioned. In the appellant's view this was not a real opportunity for providing comment. Arguments introduced in the decision under appeal by "furthermore" took about half a page, rather a lot for something that the applicant (now appellant) should understand implicitly. Moreover, the examining division had based its decision on an apparently authentic but in fact edited document in which bars had been added above the signal phi at the clock input of G3 in Figures 6 and 8. This edited document had been sent to the applicant who originally accepted it as authentic. The discrepancy between the copy of D1 sent to the applicant and the authentic published version was only discovered when the appellant was preparing the present appeal. The principle of good faith governing the relations between the EPO and applicants prohibited the examining division from basing a decision to reject an application on an aspect of a cited document that had been edited, without alerting the applicant to the editing changes before issuing the decision. The appellant conceded, however, that it was clear from a

complete study of D1 as published that the originally unidentified gate in the slave-latch circuit of Figure 8 was slave input gate G3 and the clock signal for output 0_3 of the slave input gate G3 was $\overline{phi}$.

The decision under appeal raised for the first time an objection under Article 123(2) EPC. The appellant had been given no prior opportunity to comment on this objection, either. Thus, the examining division committed a substantial procedural violation, justifying reimbursement of the appeal fee.

According to the appellant the words "transfer gate" were used in the present application to refer to both inverter-like circuits and to transmission gates.

VII. In an Annex to the summons to oral proceedings, which had been requested by the appellant, the Board required further clarification of the claimed subject-matter.

VIII. Thereupon, the appellant filed with the reply dated 9 January 1998 new claims 1 to 4 and amendments to the description.

Claim 1 is now worded as follows:

"1. An electronic flip-flop circuit having a data input (1), a data output (17) and a clock signal input (2), and comprising a first transfer gate (4) for transferring, under the control of a clock signal applied to the clock signal input, data from the data input (1) to an input (14) of a first storage element (5,6), the first transfer gate comprising a transfer transistor (4) having a main conduction channel coupled between the data input (1) and the input (14) of the first storage element (5,6) and a control electrode

receiving the clock signal, the flip-flop circuit comprising a second transfer gate (10,11,12,13) for transferring, under the control of the clock signal, data from an output (15) of the first storage element (5,6) to an input (16) of a second storage element (7,8), an output (17) of which constitutes the data output (17), the transfer gates (4,10,11,12,13) being directly driven by the same physical clock signal, characterized in that the second transfer gate (10,11,12,13) comprises a pMOS transistor (10) and an nMOS transistor (11) whose gates are connected to the output (15) of the first storage element (5,6) and whose drains are connected to the input (16) of the second storage element (7,8), the source of the pMOS transistor (10) being connected to the drain of a further pMOS transistor (12) whose source is connected to a supply voltage (Vdd) and whose gate is connected to the clock signal, the source of the nMOS transistor (11) being connected to the drain and the gate of a further nMOS transistor (13) whose source is connected to the clock signal."

Further claims 2 to 4 are dependent on claim 1.

IX. The appellant requested

(a) that the decision under appeal be set aside, the scheduled oral proceedings be cancelled and the appeal be continued in writing on the basis of the application in its present form, namely:

claims: 1 to 4 filed with the letter of 9 January 1998,

description: pages 1 to 6 as originally filed but replacing:
page 1, lines 1 to 8 as filed by the words "The invention relates to an electronic flip-flop circuit as described in the pre-characterizing part of claim 1" and
page 2, lines 2 and 3 by the words "invention is characterized by the characterizing part of claim 1";
deleting page 2, from line 8 to the period in line 15; and
inserting the acknowledgement of D1 filed with the letter of 9 January 1998 after page 1, line 25.

drawings: 1 sheet as originally filed.

(b) Reimbursement of the appeal fee;

(c) Remittal of the case to the examining division once the issue of reimbursement of the appeal fee has been decided.

Reasons for the Decision

1. The appeal is admissible.

2. *Procedural violation*

2.1 The decisions of the European Patent Office may only be based on the grounds or evidence on which the parties concerned have had an opportunity to present their comments; Article 113(1) EPC. Article 96(2) EPC in conjunction with Rule 51(2) EPC requires that the examining division shall invite the applicant, in

accordance with the Implementing Regulations and as often as necessary, to file observations, to correct the disclosed deficiencies and, where necessary, to file the description, claims and drawings in an amended form. According to Rule 51(3) of the Implementing Regulations any communication pursuant to Article 96(2) shall contain a reasoned statement covering, where appropriate, all the grounds against the grant of a European patent.

It follows therefrom that the examining division has to communicate the grounds against the grant of a patent to the applicant before refusing the application. In doing so it has to exercise its discretion to decide objectively in the light of the circumstances of each case (T 162/82, OJ EPO 1987, 533, point 12) when it is deemed necessary and appropriate to invite the applicant's comments. Although it is not necessary to give the applicant repeated opportunity to comment on the same objection (T 161/82, OJ EPO 1984, 551; T 42/84, OJ EPO 1988, 251, point 12), in a case where the applicant has made a **bona fide** attempt to overcome the objections raised by the examining division, Article 113(1) EPC may require a further offical communication dealing with the amended documents and/or the comments of the applicant.

2.2 In the present case, the examining division, in raising an objection of lack of novelty of the subject-matter of claim 1 as originally filed, argued with a list of correspondences between the subject-matter of claim 1 and the flip-flop circuit shown in Figure 8 of D1. The list did not cover all the features of claim 1: the use of the same clock signal to drive the transfer gates directly was absent. In contrast to the claimed subject-matter, D1, Figure 8, as it would be understood by the skilled person in conjunction with the description in D1, column 4, line 3 to column 5,

line 44, discloses the use of complementary clock signals for the transfer gates. The description of the present application makes it clear by distinguishing the prior art circuit shown in Figure 3 (where the clock signal driving the first transfer gate is applied in inverted form to the second transfer gate; see page 3, lines 29 to 31) from the prior art circuit shown in Figure 1 and the embodiment of the invention shown in Figure 4 (where the same physical clock signal simultaneously drives both "transfer gates"; see page 6, lines 2 and 3) that the expression "clock signal" does not cover the abstract concept of a clock signal ignoring the difference between true and inverted forms. It is limited to a clock signal in either its non-inverted **or** its inverted form (see also description page 4, lines 4 and 5). Although D1 uses the words "clock signal" in its claim 1 in a general sense, the function in the last paragraph of this claim 1, that voltage values of the control signal (phi) should be chosen such that the reading gate G1 provides an output at times other than when the reading gate G3 provides an output, emphasises the importance of the physical value (i.e. correct phase) of the clock signal.

It is therefore clear, that the applicant (appellant) could not understand the lack of novelty objection in the communication dated 11 April 1995 and expressed this in his reply dated 28 July 1995. The observations concerning the feature "the transfer gates being directly driven by the same clock signal" and the suggested insertion of a definition of the term "transfer gate" into the description must be considered to represent a **bona fide** attempt to overcome the objections concerning lack of novelty of the subject-matter of claim 1 and unclear terminology. The feature "the transfer gates being directly driven by the same clock signal" in claim 1 was not dealt with expressis

verbis in the only communication issued by the examining division, but only in the contested decision. The same applies to the refused insertion of the definition of the term "transfer gate" into the description. Thus the appellant did not have an opportunity to present his comments with regard to the grounds for refusal before the decision to refuse the application was issued. The giving of such an opportunity is mandatory in accordance with Article 113(1) and Article 96(2) and Rule 51(2) and (3) EPC.

2.3 Thus the examining division committed a substantial procedural violation, which means the contested decision must be set aside and the case remitted to the examining division for further examination of the application (Article 10 of the Rules of Procedure of the Boards of Appeal, OJ EPO 1980, 171). This means here resumption of the examination on the basis of the request filed with the letter dated 9 January 1998. It is left to the examining division to decide whether these new documents meet the requirements of the EPC.

2.4 The following questions should be considered:

(a) whether the type of the first transfer transistor (4) should also be defined in claim 1, in view of the desired same physical clock signal.

(b) whether the prior art according to Figure 3 may be more relevant for the claimed subject-matter than the Figure 1 prior art in view of the NMOS transistor used for the first transfer gate in Figures 3 and 4 and in view of the fact that the second transfer gate of Figure 4 is a complex circuit in which the proper transfer circuit (inverters 10 and 11, see page 6, lines 5 and 6 of the description) is triggered by an intermediate

delaying circuit (transistors 12 and 13). In doing this, it may be necessary to examine whether in the prior art circuit of Figure 3 the second NMOS transistor with the intermediate inverter could also be considered to be a "transfer gate" in view of the broad definition used in the present application. This may have consequences in connection with Rules 27(1)(c) and 29(1) EPC.

2.5 Constructive suggestions such as presented in paragraphs 3 and 4 of the communication of the examining division may be useful when accompanied by properly substantiated objections. An objection under Article 84 EPC against original claim 1, e.g. concerning the words "prolonging the transfer time", "clock signal" and "second transfer gate" may have been appropriate.

2.6 Regarding the use of the edited document D1, it goes without saying that care should always be taken to ensure that only authentic documents (as published) are cited and sent with official communications. This applies even if the editing concerns the correction of an obvious error in a cited document. This is even more important in cases where a manual amendment is not clearly recognisable as such, e.g. inverting bars above a symbol.

3. Since the Board has found a substantial procedural violation to be the ground for allowing the appeal, it finds it appropriate to order reimbursement of the appeal fee in accordance with Rule 67 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance for further prosecution of the application as indicated in paragraph IX and taking account of paragraphs 2.3 and 2.4 above.

3. Reimbursement of the appeal fee is ordered.

The Registrar:

M. Kiehl

The Chairman:

W. J. L. Wheeler