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D E C I S I O N
of 29 May 2001

Case Number: T 0070/96 - 3.4.3

Application Number: 90830428.0

Publication Number: 0478871

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:
Formation of contact plugs by blanket CVD deposition and etchback

Applicant:
STMicroelectronics S.r.l.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 123(2)

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

Case Number: T 0070/96 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 29 May 2001

Appellant: STMicroelectronics S.r.l.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 4 September 1995 refusing European patent application No. 90 830 428.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
M. B. Günzel

Summary of Facts and Submissions

I. The appeal lies from the decision of the examining division dated 4 September 1995, to refuse European patent application No. 90 830 428.0 on the grounds that the invention as claimed does not meet the requirements of Articles 52(1) and 56 EPC.

The decision of the examining division is based on the following documents:

D1: DE-A-3 636 547

D2: EP-A-0 245 627

II. The notice of appeal was filed, and the appeal fee paid, on 24 October 1995, and the statement of grounds was filed on 27 December 1995.

III. The appellant requests that the decision of the examining division be set aside and that a patent be granted on the basis of the following documents:

Claims: 1 to 7 as filed on 10 March 1995

Description: pages 1 to 3, 5 to 7, 10 as originally filed on 1 October 1990
pages 4, 4bis, 8, 9as filed on 8 September 1994

Drawings: Figures 1 to 3 (Sheet 1/3) as originally filed on 1 October 1990
Figures 4a-d (Sheet 2/3) and
Figures 5a-f (Sheet 3/3)as filed on

8 September 1994

The appeal is thus based on the same set of claims as the decision of the examining division. There are no auxiliary requests.

IV. Claim 1 of the appellant's request reads as follows:

"1. A process for forming contacts with a semiconducting substrate (3) and/or interconnection vias between a first conducting layer (4) and a second conducting layer to be formed at a higher level than said first conducting layer (4), comprising forming conducting plugs (1p) of a metallic material by filling contact and/or via holes, formed through an isolation layer (2) of a dielectric material formed over said semiconducting substrate (3) and/or over said first conducting layer (4), by blanket chemical vapor deposition of a metallic matrix layer (1) comprising at least a filling layer of a metallic material chemically deposited from vapor phase, and etching back said chemically deposited matrix layer (1) for removing it from the surface of said isolation layer (2) of dielectric material while leaving said conducting plugs (1p) in the respective holes, characterized by the fact that the process comprises the following steps:

arresting the anisotropically etching back of said filling layer (1) of said chemically deposited metallic material when the surface of the underlying dielectric material (2) onto which said first metallic material (1) has been deposited is exposed while leaving plugs (1p) of said filling metallic material within said holes and residues (1r) along discontinuities from planarity of said surface;

masking with caps (5) of a masking material said

plugs (1p);

overetching said filling metallic material (1) for eliminating said residues (1A) on the unmasked surface of said underlying dielectric material (2) under conditions of reduced anisotropy and increased etch selectivity of said filling metallic material of said matrix layer (1) versus said dielectric material of said dielectric layer (2), as compared with said first etchback step."

The remaining claims 2 to 7 are directly or indirectly dependent from claim 1.

V. The arguments put forward by the appellant in support of the application can be summarised as follows:

The choice of document D1 as the closest prior art for assessing whether the invention involves an inventive step, is based on a misconception. It is clearly impossible to employ thermally grown polysilicon crystals to realise vias, since their contact resistance is orders of magnitude greater than normally acceptable values, the temperature involved in growing the silicon is also far too high and the technique requires the underlying layer to be monocrystalline silicon (statement of grounds, page 1, last four paragraphs).

The closest prior art for judging whether the claimed invention involves an inventive step is document D2, which relates to the known tungsten-plug process as represented in the introduction to the description in the application in suit and the preamble of claim 1 (statement of grounds, page 4, paragraph 5).

Taking document D2 as the closest prior art, there is nothing in the prior art which would induce the skilled person to divide the etching of the tungsten layer into two distinct phases and to separate those phases by an intermediate step of masking the plug areas, all for overcoming a problem in a subsequent aluminium sputtering step (statement of grounds, page 4, paragraph 6).

Reasons for the Decision

1. The appeal is admissible.

2. *Alllowability of amendments under Article 123(2) EPC*

2.1 Claim 1 in its present form differs in substance from claim 1 as originally filed only by the features stated in the last paragraph of the claim. These features correspond to the features originally claimed in claim 2. The remaining differences are of a minor nature and in the Board's judgement do not introduce matter going beyond the subject matter of the application as filed. The amendments are therefore admissible under Article 123(2) EPC.

3. *Inventive Step*

3.1 The invention concerns a method of providing, in integrated circuits, contacts and interconnections between wiring layers by means of metallic plugs which are formed as follows. Holes are formed in a dielectric layer and are filled with metallic material by blanket chemical vapour deposition of a metallic layer. The

metallic layer is then etched back anisotropically. When the etching exposes the surface of the dielectric layer, the holes remain filled by the conducting metallic plugs but there are also residues of the metallic layer left along surface discontinuities of the dielectric layer. To remove the residues, anisotropic etching is halted, the plugs are masked and etching is resumed under conditions which differ from the preceding etching step by reduced anisotropy as well as by increased etch selectivity of the metallic material as compared to the material of the dielectric layer.

3.2 The closest prior art

3.2.1 In the decision under appeal, document D1 was regarded as the closest prior art. Document D1 discloses the formation of conductive plugs in the following manner: An insulating layer is deposited on a silicon substrate, and contact holes are opened up in the insulating layer. A layer of aluminium alloy containing silicon and a p-type dopant is deposited by blanket deposition on the insulating layer and in the contact holes. The alloy has a higher than normal silicon content so that silicon easily precipitates out of the alloy (column 3, lines 27 to 32). During a subsequent heat treatment, silicon precipitates primarily where the alloy is in contact with the silicon of the substrate, that is, inside the contact holes. By epitaxial growth from the solid phase, the contact holes are filled with p-doped silicon (column 3, lines 33 to 39) which forms the conducting plug. The aluminium alloy layer is then removed from the surface of the insulating layer by etching, which exposes not only the silicon plugs in the contact holes but also

unwanted precipitates of silicon formed on the surface of the insulating layer. To remove these unwanted precipitates, a patterned mask is applied to cover and protect the silicon plugs and then the silicon residues are removed in a further etching step.

It follows from the foregoing that the method known from document D1 is exclusively for the selective epitaxial growth of silicon plugs. Hence, a skilled person concerned with providing metallic plugs would not consider the teaching of document D1 to be relevant to this end. The Board therefore accepts the appellant's argument that document D1 is not the appropriate closest prior art, and concludes that the objective problem which had been defined on the basis of this prior art document as being the provision of a conductive plug with a lower resistivity than a doped semiconductor, is also not appropriate.

3.2.2 Document D2 on the other hand teaches a process of forming metallic plugs in semiconductor circuits, which has the following features:

(i) a tungsten layer is deposited on an insulating layer (2) by chemical vapour deposition. Because tungsten is deposited on the bottom and the sides of the holes (column 2, lines 11 to 27), the holes are filled at a rate faster than the rate of vertical blanket deposition. Nevertheless, when deposition is complete, depressions are still left in the surface of the tungsten layer where the holes have been filled (Figure 1).

(ii) An organic layer is deposited on the tungsten

layer. Being spun on (column 3, lines 35 to 37), the top surface of the organic layer is essentially planar, which means that the organic layer is thicker above the depressions in the surface of the tungsten layer than elsewhere (layer 6 of Figure 1). As shown by of Figure 2, anisotropically etching the organic layer back to the tungsten surface results in islands (6a) of organic material being left behind where the organic layer was thickest, that is, on top of the conductive plugs (5a). Hence, the islands (6a) form masks which are self-aligned with respect to the tops of the plugs (col. 2, lines 51 to 54, col. 3, lines 38 to 49 and Figure 2).

(iii) Next, the blanket layer of tungsten material is selectively etched back wherever the tungsten surface is not covered by a mask, until the insulating layer (Bor-Phosphor-Silikatglasschichtoberfläche 2) is exposed (column 3, lines 1 to 3 and lines 49 to 52).

(iv) After the tungsten layer has been removed by etching everywhere except for the masked plugs, the organic material masking the plugs is removed (column 4, lines 1 and 2).

According to document D2, the technique aims, inter alia, to ensure that the insulating layer is free of tungsten residues (column 2, lines 38 and 39).

The process disclosed in document D2 and the process claimed in claim 1 of the invention in suit both use conductive plugs formed from metallic material

deposited on the surface of an insulating layer by blanket chemical vapour deposition. Both processes are capable of providing electrical connections to an underlying metal layer. Although different steps are taken in the two methods to remove all the unwanted metal yet leave the conductive metal plugs intact, in both cases the deposited metal layer is etched back until only the metallic plugs remain which fill the contact holes. In view of the basic similarities of the processes as claimed in the application in suit and as disclosed in document D2, the Board concludes that of the cited documents document D2 constitutes the closest prior art for the purpose of assessing whether the claimed invention involves an inventive step.

3.3 The objective problem and its solution

Starting from the closest prior art, document D2, the objective problem addressed by the invention is therefore to provide an alternative manner of forming metallic conductive plugs by chemical vapour deposition of the metallic material.

As set out in full in the characterising portion of claim 1, the invention solves this problem by applying the following measures during etching off excess metallic material:

(a) anisotropic etching of the metallic layer (1) is arrested when the surface of the underlying dielectric layer (2) is reached. At this point, the conducive plugs still fill the holes and residues of the metallic material remain along discontinuities in the planarity of the surface of the dielectric layer,

(b) the conductive plugs are masked with caps (5), and

(c) the unmasked residues of the metallic material are etched under conditions of reduced anisotropy and increased etch selectivity to remove them from the surface of the underlying dielectric material.

In summary, the claimed method thus employs two etching steps, (a) and (c), separated by a step b) of masking the plugs. Most of the metal is removed in the first etching step using anisotropic etching, while the second etching step serves to remove under different etching conditions any residues which have been left behind by the first step.

In contrast, in the method disclosed in document D2 the plugs are masked prior to the start of the single etching step which removes all unwanted metal without leaving any residues. There is nothing in document D2 which would indicate to the skilled person that metallic residues which require removing would be left behind when the metallic layer is anisotropically etched until the surface of the insulating layer is reached. Document D2 therefore cannot of itself make the claimed invention obvious.

The formation of unwanted residues of silicon, and their removal, is described in document D1. The method disclosed in document D1 involves two different etching steps, the first for removing the alloy layer and the second for removing the silicon residues, and these two etching steps are separated by an intermediate masking step to protect the conducting plugs. In order to consider whether the skilled person would contemplate combining this teaching of document D1 with that of the

closest prior art document D2, the following points must be taken into account:

(i) The plugs formed by the methods in document D1 and in document D2 are markedly different; they are, respectively, of silicon which has been grown *in situ* from an alloy and of metal which has been deposited by chemical vapour deposition.

(ii) according to document D1, residues are formed randomly on the surface of the underlying insulating layer through precipitation of silicon from the deposited aluminium-silicon alloy and are exposed by etching back the alloy; the method of document D2 does not leave any residues.

(iii) In the method disclosed in document D1, a mask is applied only after the silicon-aluminium alloy has been removed by the first of two etching steps; in document D2, a mask is formed before there is any etching of the tungsten layer. On the basis that document D2 describes the next stage of processing to be the formation of a further metallisation layer (column 4, lines 3 to 6), the method of document D2 involves removing the masking material only after all the unwanted tungsten has been removed. In these circumstances, what is disclosed in document D1 could not simply be applied to the method as it is described in document D2 without significant modification of the latter.

In summary, as regards the disclosures in documents D2 and D1, there are differences in the materials employed and differences in the way they are processed, as well as the absence of residues in the method of document D2. As there are no residues, the skilled person has no reason to introduce into the method of document D2 an intermediate masking step and a further etching step as taught by document D1. Moreover, neither of the two documents contains any incentive to consider modifying the method of document D2 in this manner. The Board therefore concludes that the skilled person would not combine the contents of document D2 and D1 when trying to solve the objective problem defined in the first paragraph of this section.

3.4 Taking into account the facts and arguments set out above, it is the Board's judgement that the invention as claimed in claim 1 is not obvious from the contents of the prior art documents D2 and D1 and, hence, that it involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant the patent on the basis of the documents listed in paragraph III of this decision.

The Registrar: The Chairman:

L. Martinuzzi R. K. Shukla