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D E C I S I O N
of 23 September 1998

Case Number: T 0040/96 - 3.5.1

Application Number: 86117469.6

Publication Number: 0226205

IPC: G06F 11/20

Language of the proceedings: EN

Title of invention:
Method of relocating data in and extending life of a memory system

Patentee:
Pitney Bowes Inc.

Opponent:
Neopost Ltd
Francotyp-Postalia Aktiengesellschaft & Co.

Headword:
-

Relevant legal provisions:
EPC Art. 52(1), 56, 100(a), 114(2)

Keyword:
"Inventive step (no)"
"Late filed document"

Decisions cited:
T 0156/84

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0040/96 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 23 September 1998

Appellant: (Opponent I)
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Decision under appeal: **Decision of the Opposition Division of the European Patent Office posted 15 November 1995 rejecting the opposition filed against European patent No. 0 226 205 pursuant to Article 102(2) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: A. S. Clelland
C. Holtz

Summary of Facts and Submissions

I. This appeal is against the decision of the opposition division to reject an opposition against European patent No. 0 226 205, the opposition division taking the view that the subject-matter of claim 1 was both novel and inventive. Inter alia the following documents, submitted by the two opponents with their notices of opposition, were cited in the decision:

D11: US-A-3 668 644

D21: US-A-3 544 777

D23: H. Kopetz: "Softwarezuverlässigkeit", published by Hanser, Munich & Vienna, 1976

D24: DE-A-31 27 349

D25: DE-A-29 07 333

II. In the course of the proceedings opponent II submitted the following additional document:

D26: IEE Proceedings, Vol. 128, Pt. A, No. 4, May 1981, pages 257 to 272, P.G. Depledge: "Fault-tolerant computer systems".

This document was submitted on 22 September 1995, shortly before the oral proceedings before the opposition division on 12 October 1995 and after expiry of both the opposition period (Article 99(1) EPC) and the one-month time limit set by the opposition division for the preparation for the oral proceedings (Rule 71(a)(1) EPC).

III. On 11 January 1996 the appellant (opponent II) lodged an appeal against the decision and paid the prescribed fee. A statement of grounds of appeal was subsequently filed.

IV. At oral proceedings before the Board the appellant requested that the decision under appeal be set aside and the patent revoked. The respondent requested that the appeal be dismissed and the patent be maintained as granted, or alternatively that the patent be maintained on the basis of claims 1 to 11 and an amendment to column 14 of the patent description, as submitted on 14 August 1998.

V. Claim 1 of the granted patent reads as follows (omitting reference signs):

"1. A method of relocating data stored in a memory bank comprising the steps of:
(a) partitioning said memory bank at least a first memory part, a second memory part and third memory part;
(b) storing first data in said first memory part; and
(c) storing second data in said second memory part, said second data duplicating said first data;
characterized by the step of:
(d) writing and storing one of said first data or said second data stored in said first or said second memory part upon determination of error in the other in said third memory part whereby said data in one memory part is duplicated in said third memory part in substitution for the corresponding data stored in the other of said memory parts."

Claim 1 of the auxiliary request differs in substance from claim 1 of the main request in being limited to a method of relocating data stored in a **single** memory bank.

VI. The appellant and opponent I argued as follows:

Document D26 was a reference article which surveyed the available techniques of hardware redundancy; it therefore represented the common general knowledge in the art and should be admitted to the proceedings. Furthermore, it was more relevant than any of the other prior art documents because it disclosed in connection with Figure 6 the idea of combining active and passive redundancy, which was the core idea of the patent.

Even if D26 were to be left out of consideration, the subject-matter of claim 1 of the main request was obvious in view of the disclosure of D21. First, D21 suggested the automatic replacement of the failed memory; this technique was well known per se, as exemplified by the paragraph bridging pages 7 and 8 of D24. Secondly, a memory could only function when provided with data; copying the valid data from the good memory into the standby memory was therefore an obvious expedient. D21 referred to returning the system to "two memory operation" which implied that the memories contained the same data. It did not make sense to use a backup as the source of data for the standby memory because, unlike the data in the other memory, backup data would not always be up to date.

The limitation in the auxiliary request was of unclear effect. Furthermore, the division of a single memory into parts was well known and the use of these different parts when errors occurred was described in general terms in the textbook extract D23 at page 126, paragraph 2 and exemplified in D25 beginning at page 11.

VII. The respondent argued as follows:

Document D26 was submitted late; the opposition division was correct in not admitting it into the proceedings and it should not be admitted now. Even if relevance were the only criterion for admissibility, it should not be admitted because it did not relate specifically to memories and was less relevant than D21.

It was accepted that D21 disclosed the replacement of a failed memory in a two-memory redundant memory system. It did not however disclose automatic replacement of the failed memory. From the description at column 3, lines 25 to 30 it was apparent that switching means were operated by a maintenance engineer when the system indicated which circuit had failed. The art took the view that the automatic substitution of failed elements was not a good idea because complicated switching circuits were prone to error, as could be seen from D24 at the paragraph bridging pages 7 and 8. Secondly, since D21 did not describe how the replacement memory was used, it could not suggest the claimed remapping process. In fact, remapping was not possible in the system of D21 because Figure 4 showed that the central processor could only write to the two memories simultaneously. Thus, if anything, D21 suggested copying the data simultaneously into the two memories, as was the usual practice in the art, to return a memory to normal operation. It seemed probable that this data was derived from backup data from elsewhere in the system. The document nowhere suggested that data stored in the operational memory part was written into and thus duplicated in the newly introduced memory part, in substitution for that in the failed memory part.

Claim 1 of the auxiliary request covered the preferred idea of partitioning the memory by sub-dividing a single memory. This had the advantage when applied to non-volatile memory (NVM) units of increasing their life, which was normally limited by the number of read/write cycles. This was achieved by remapping data in a single memory bank when a particular area in an NVM unit failed. D21 related to core memories which did not show this type of failure. There was no suggestion in any of the cited documents of using a remapping process in a single memory.

Reasons for the Decision

1. The appeal complies with Article 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. *Late-filed Document*

2.1 As will be apparent from point II above, D26 was late-filed. In accordance with Article 114(2) EPC the EPO may disregard facts or evidence which are not submitted in due time by the parties concerned. In the case of opposition proceedings the due time is within the 9 month term. The opposition division and the Board accordingly have a discretion under Article 114(2) EPC to exclude D26. However, the Board may consider under Article 114(1) EPC whether D26 is of such relevance as to justify its admission to the proceedings at a late stage.

2.2 D26 is a review article which discusses the principles of fault-tolerant computer techniques. Although ostensibly introduced to exemplify the common general knowledge in the art, it was put forward at the oral

proceedings as the closest prior art. Figure 6 and the associated text were cited as disclosing the idea of combining active and passive redundancy, referred to as hybrid redundancy, see point 3.1 below.

2.3 However D26 is of such generality that the Board is unable to identify specific features which make it more relevant than other documents already in the proceedings; it does not, for example, explicitly refer to a redundant memory system.

2.4 The Board therefore takes the view that D26 should not be admitted into the proceedings (Article 114(2) EPC).

3. *Inventive step (main request)*

3.1 In accordance with the description, the problem to be solved by the patent is that of increasing the service life of a postal meter by extending the life of a non-volatile memory used in it. The memory is divided into at least two parts containing identical data, providing what is known in the art as active redundancy. If an error is determined in the data in either of these memory parts, the data from the other part are copied into a standby (third) memory part. The use of a standby memory is known in the art as passive redundancy. Although not mentioned in the patent it was asserted by the respondent that a particular kind of non-volatile memory has a limited life, dependent on the number of read/write cycles. In such a memory only part may in fact be in use, and only this part may fail. By partitioning the memory and storing identical data in two separate partitions, i.e. address regions, failure in one partition may be overcome by remapping or readdressing the data to a third partition. This process can be repeated for successive partitions until the whole memory has been used up.

3.2 Claim 1 of the main request is not however limited to a single non-volatile memory but is more broadly expressed as a method of relocating data stored in a "memory bank" which is partitioned into three parts. The Board notes that the expression "memory bank" is of vague scope and has looked to the description for clarification. Column 14, lines 45 to 54 of the description includes the following passage:

"...it will be apparent that a plurality of memory banks maybe [sic] used where one memory bank serves as the primary bank... a second memory bank serves as a secondary bank... and additional memory banks are provided to serve as reserve memory banks for the purpose of remapping."

Claim 3 as granted, which is appendant to claim 1, explicitly claims an arrangment in which "said memory bank includes a plurality of memory banks". The Board accordingly concludes that the expression "memory bank" should be interpreted as embracing both a single memory and a plurality of memories.

3.3 In the course of the oral proceedings it became apparent that the single most relevant document is the acknowledged prior art document D21. Figure 1 of D21 discloses a memory system in which the memory is partitioned into two parts, 12 and 14; identical data is stored in the two parts. A failure analysis subsystem 30 detects a difference in the outputs of the memory parts and switches the system to a failure analysis mode in which the failed memory is determined and, in the main embodiment, switched out of operation. The system continues in operation with the operational memory part.

3.4 In accordance with column 2, line 69 to column 3, line 30 of D21 the failed memory can be repaired or

replaced; column 3, lines 28 to 30 envisages an embodiment in which the repair means comprise "a switching means which functions to substitute spare circuits for failed circuits". It was common ground at the oral proceedings that this passage refers to the replacement of a defective memory part by a further memory part. The respondent argued however that D21 did not disclose automatic replacement and was silent as to how the data for the newly introduced memory part was derived. It was probable that the data would be provided by an independent back-up device.

3.5 The Board notes from the cited passage that the use of a switching means to substitute a spare circuit for a failed circuit is considered an alternative to an indication to a maintenance man as to which circuit has failed. This strongly suggests that the substitution is indeed carried out automatically.

3.6 As regards the origin of the data in the substitute memory, it appears to the Board that this depends on the nature of the data; if the data is not important, clearing both memories and restarting the process to return to two-memory operation would be possible. If the data is of secondary importance, for example text input to a word processor, it would be adequate to copy the data from a backup device as suggested by the respondent. If, however, the data is very important, c.f. "certain critical data processing system applications" as mentioned in D21 at column 2, lines 34 to 37, a backup from an earlier time may not be good enough. The system could only "continue to operate after only a short delay" as envisaged by D21 at column 2, lines 67 and 68, if the most recent data, namely the data in the good memory, were used. Thus even if D21 does not explicitly show that the two memories can be written to separately, one obvious solution to the problem of restarting operation with

the substitute memory would be to copy the data from the good memory into the substitute memory.

3.7 The skilled person carrying out the teaching of D21 and making use of the embodiment envisaged at column 3, lines 28 to 30 would thus without the exercise of invention arrive at a method of relocating data stored in a memory bank in accordance with claim 1. The subject-matter of the claim therefore lacks an inventive step.

4. *Inventive step (auxiliary request)*

4.1 Claim 1 of the auxiliary request limits the expression "memory bank" to a "single memory bank", in other words, rather than embracing both a plurality of discrete memories and a single memory, the claim is now intended to be restricted to the latter. The passage at column 14, lines 45 to 54 quoted at point 3.2 above has been deleted.

4.2 It is not wholly clear to the Board that the intention in fact succeeds; as noted at point 3.2 above the patent nowhere defines what is meant by a "memory bank". Even after deletion of the broadening passage in the description the term is not so clear in itself as to exclude a memory made up of a plurality of discrete memories.

4.3 Even if for the sake of argument the respondent's interpretation is accepted, it is observed that the claim is not limited to any particular kind of memory. The question therefore arises as to whether the skilled person would be led to apply the teaching of D21 to a single device. The respondent argues that this is not the case because in D21 both memories have identical addresses and are addressed simultaneously, whereas in the case of a single memory two separate sets of addresses are necessary. It is argued that the skilled person would not derive this from D21.

4.4 The reconfiguration of memory devices to exclude defective portions was at the claimed priority date common general knowledge. Thus D23, which is an extract from a textbook published in 1976, states at page 126 that in systems with virtual addressing a defective main memory block can easily be worked around ("Ebenso läßt sich in Systemen mit virtueller Adressierung ein fehlerhafter Hauptspeicherblock relativ einfach umgehen"). Moreover, from well before the claimed priority date the semiconductor device art has evinced a continuous trend towards reduction of the number of discrete components and their integration, so that the skilled person would at the claimed priority date have appreciated that the discrete components of Figure 1 of D21 could be integrated on a single chip. Given the common general knowledge exemplified by D23 that defective memory portions can be isolated, no technical prejudice would appear to exist against doing so. The Board accordingly concludes that the skilled person would without the exercise of invention have integrated the components of Figure 1 of D1, including both memories and any spare memory parts, on a single chip and made provision for switching to the spare memory parts as needed. The subject-matter of claim 1 of the auxiliary request accordingly lacks an inventive step.

5. There being no other requests, it follows that the patent must be revoked.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The patent is revoked.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg