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D E C I S I O N
of 2 December 1999

Case Number: T 0898/95 - 3.4.3

Application Number: 91308647.6

Publication Number: 0478262

IPC: H01L 21/82

Language of the proceedings: EN

Title of invention:
Random access memory device and process of fabrication thereof

Applicant:
NEC Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Novelty (after amendments: yes)"
"Inventive step (yes) - cause of an obvious problem not apparent from the prior art"

Decisions cited:
-

Catchword:
-

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Case Number: T 0898/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 2 December 1999

Appellant: NEC Corporation
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Minato-ku
Tokyo (JP)

Representative: Abnett, Richard Charles
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 23 May 1995 refusing European patent application No. 91 308 647.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 91 308 647.6 (publication No. 0 478 262) was refused in a decision of the examining division dated 23 May 1995 on the ground that the subject-matter of claims 1 and 2 forming the basis of the decision lacked novelty having regard to document

D1: Patent Abstracts of Japan, vol. 14, No. 257, (E-936) [4200] & JP-A-2 077 154.

II. The applicant lodged an appeal against this decision on 21 July 1995 paying the appeal fee on the same day. The statement of the grounds of appeal was filed on 22 September 1995.

III. During the oral proceedings held before the Board on 2 December 1999 the appellant filed a new set of 11 claims, the only independent claims 1 and 5 having the following wording:

"1. A random-access memory device fabricated on a single semiconductor substrate (21; 41; 61) of a first conductivity type, comprising:

a) a plurality of memory cells; and

b) at least one component field-effect transistor forming a part of a peripheral circuit;

in which each of said plurality of memory cells comprises:

a-1) a transfer field-effect transistor having first and second lightly-doped impurity regions (26b/26a; 47b/47a; 67b/67a) of a second conductivity type

opposite to said first conductivity type spaced apart from each other by a first channel-forming region, a first gate insulating film (24; 44; 64) formed on said first channel-forming region, and a first gate structure (25a; 46a; 66a) formed on said first gate insulating film,

a-2) a first inter-level insulating film (27; 48; 68) covering said first gate structure and exposing said first and second impurity regions, and

a-3) a stacked-type storage capacitor having a lower electrode (28; 50; 70) formed on said first inter-level insulating film and held in contact with said first lightly-doped impurity region, a dielectric film structure (30; 52; 72) covering said lower electrode, and an upper electrode (31; 53; 70) held in contact with said dielectric film structure;

in which said at least one component field-effect transistor comprises:

b-1) third and fourth impurity regions of said second conductivity type spaced apart from each other by a second channel-forming region, each of said third and fourth impurity regions being implemented by a lightly-doped impurity sub-region (26c; 47c; 67c) partially overlapped with a heavily-doped impurity sub-region (34; 55a; 75a),

b-2) a second gate insulating film (24; 44; 64) formed on said second channel-forming region, and

b-3) a second gate structure (25c; 46c; 66c) formed on said second gate insulating film and having side walls (32b; 49c; 69c) on side surfaces thereof, said side walls being made from an insulating film used for said first inter-level insulating film;

and in which:

a-4) each of said plurality of memory cells does not comprise a heavily-doped impurity sub-region having a dopant level corresponding to said heavily-doped impurity sub-region of said at least one component field-effect transistor;

and said random-access memory device further comprising:

c) an upper inter-level insulating film structure (35/37; 56/58; 76/79/82) covering said plurality of memory cells and said at least one component field-effect transistor and having contact holes exposing said second impurity region and one of said third and fourth impurity regions, and

d) conductive wiring strips (36; 57; 81/80a) passing through said contact holes and held in contact with said second impurity region and said one of said third and fourth impurity regions, respectively."

"5. A process of fabricating a random-access memory device, comprising the steps of:

a) preparing a semiconductor substrate (21; 41; 61) of a first conductivity type;

b) forming first and second gate structures (25a/25c; 66a/66c; 66a/66c) on first and second gate insulating films, respectively;

c) forming first and second lightly-doped impurity regions and third and fourth lightly-doped impurity sub-regions (26b/26a/26c; 47b/47a/47c; 67b/67a/67c) of a second conductivity type in a self-aligned manner by ion implantation using said first and second gate

structures as a mask, said second conductivity type being opposite to said first conductivity type, a transfer field-effect transistor being completed with said first gate structure and said first and second lightly-doped impurity regions;

d) covering said first and second gate structures with a first inter-level insulating film (27/48; 68);

e) forming a stacked-type storage capacitor (28/30; 31; 50/52; 53; 70/72/73) provided on said first inter-level insulating film and held in contact with said first lightly-doped impurity region;

f) anisotropically etching said first inter-level insulating film covering said second gate structure so that side walls (32b; 49c; 69b) are formed on side surfaces of said second gate structure;

g) forming heavily-doped impurity sub-regions (34; 55a; 75a) of said second conductivity type in a self-aligned manner by ion implantation using said second gate structure and said side walls as a mask, said heavily-doped impurity sub-regions being partially overlapped with said third and fourth lightly-doped impurity sub-regions, respectively, thereby completing a component field-effect transistor forming a part of a peripheral circuit, whilst covering said transfer field-effect transistor with a mask layer (33) so that the transfer field-effect transistor comprises lightly-doped regions only without heavily-doped regions;

h) completing an upper inter-level insulating film structure (35/37; 56/58; 76/79/82) covering said transfer field-effect transistor, said stacked-type storage capacitor and said component field-effect transistor; and

i) completing conductive wiring strips (36; 57; 80a/81) respectively held in contact with said second lightly-doped impurity region and one of said heavily-doped impurity sub-regions through respective contact holes formed in said upper inter-level insulating film."

Present claim 1 differs in substance from claim 1 of the set of claims forming the basis for the decision under appeal in that it comprises additionally the feature (a-4) that each of the plurality of memory cells does not comprise a heavily-doped impurity sub-region having a dopant level corresponding to the heavily-doped impurity sub-region of the at least one component field-effect transistor.

Present claim 5 differs in substance from the corresponding independent process claim of the set of claims forming the basis for the decision under appeal in that,

in step (g), it is specified additionally that the step of heavily doping is effected whilst covering the transfer field-effect transistor with a mask layer (33) so that the transfer field-effect transistor comprises lightly-doped regions only without heavily-doped regions,

and in that,

in step (c), it is specified that the transfer field-effect transistor is completed with the first gate structure and, additionally, with the first and second lightly-doped impurity regions.

Claims 2 to 4 and 6 to 11 are dependent on claims 1 and 5, respectively.

IV. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims filed during the oral proceedings with the description to be adapted, as main request, or, subsidiarily, on the basis of the subsidiary requests 1 to 3 contained in his letter dated 24 November 1999.

V. The appellant submitted essentially the following arguments in support of his main request:

Claim 1 is distinguished from the memory device in document D1 in that the stacked capacitor according to claim 1 is in contact with the lightly-doped impurity region of a transfer transistor and not with a heavily-doped sub-region as in the device of document D1. Moreover, there is no heavily-doped region overlapping the lightly-doped region in the transfer transistor.

In the RAM device of document D1, the field-effect transistors of the memory cells and those of the peripheral circuit are of the LDD (lightly-doped drain) type, i.e. the transistor having lightly-doped impurity sub-regions which are partially overlapped with heavily-doped impurity sub-regions.

The present inventor was the first to recognize that the RAM devices of document D1 had a drawback in that, as derivable from the application as filed (see in particular page 5, third paragraph in combination with the description of the prior art illustrated by Figures 1A and 1B), a data bit or electrons stored in the lower electrode of the storage capacitor in contact with a highly-doped region of the memory cell transistors were lost in relatively short time period; this was because of the fact that the heavily doped source and drain regions were liable to be formed in

damaged areas caused by the anisotropical etching process for patterning the side walls which are necessary for forming the heavily-doped impurity sub-region partially overlapping the lightly-doped impurity sub-region of the LDD doped regions.

To solve this particular problem, the invention is distinguished over the RAM devices known from document D1 in that, in the memory cells, doped regions which are not of the LDD type and thus are different from those of the peripheral circuit part, are implemented, as specified in feature (a4) of claim 1.

The inventiveness of the claim may be supported by the fact that the improvement over document D1 might be initially considered by the skilled person as a retrograde step. Usually, in the interest of increased integration, it is considered desirable to replace "standard" transistors having single doping levels, by smaller LDD transistors. The present inventor has recognized that an improvement to the "all-LDD" structure of document D1 may be made by replacing LDD structures in selected positions within the RAM device (i.e., not beneath component transistors, but only beneath transfer transistors of the memory cells), to produce a novel and advantageous structure providing an improved retention of data bits provided by a single doping-level structure.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 Admissibility of the amendments

Present claim 1 specifies in features (a1) and (a3) that the first and second impurity regions (26b/26a; 47b/47a; 67b/67a) of the second conductivity type of the transfer field-effect transistor of each memory cell are lightly-doped, and specifies in feature (a4) that each of the plurality of memory cells does not comprise a heavily-doped impurity sub-region having a dopant level corresponding to the heavily-doped impurity sub-region of the at least one component field-effect transistor. These features, which are not recited in claim 1 as filed, are derivable from the whole content of the application as filed (see in particular the devices in Figures 2E, 3F and 4H; see in particular page 13, antepenultimate line to page 14, fifth line).

In this respect, as convincingly argued by the appellant, the problem solved by the invention as presently claimed is also clearly derivable from page 5 of the application as filed.

Present claim 5 specifies in step (g) that heavy doping is effected whilst covering the transfer field-effect transistor with a mask layer (33) so that the transfer field-effect transistor comprises lightly-doped regions only without heavily-doped regions, and, in step (c), that the transfer field-effect transistor is completed with the first gate structure and the first and second lightly-doped impurity regions. These features, which

are not recited in the independent process claim as filed, i.e. claim 2, are derivable from the whole content of the application as filed (see in particular Figures 2A to 2E, 3A to 3F and 4A to 4H; see also the statement of the process of the invention, page 8, last paragraph to page 9, first paragraph).

Present claims 2 to 4 and 6 to 11 are dependent on present claims 1 and 5, respectively; they concern particular embodiments of the device and of the process of fabrication, respectively, which have a basis in particular in the drawings and the corresponding text locations of the description in the application as filed.

Therefore, in the Board's judgement, the present application satisfies the requirement of Article 123(2) EPC that a European patent application may not be amended in such a way that it comprises subject-matter which extends beyond the content of the application as filed.

2.2 Clarity

Feature (a4) of present claim 1, together with other features of the claim, specify that, contrary to the component field-effect transistors of the peripheral circuit of the D-RAM device, the field-effect transistors of the memory cells are not of the LDD-type.

Features (g) and (c) of present independent claim 5 together express in process terms the same technical feature.

The main claims are in the one-part form. This is considered to be justified in the interest of an unambiguous definition of the invention in view of the multiple clarity objections concerning formerly submitted claims, expressed by the Board in the annex to the summons to oral proceedings (Rule 29(1) EPC).

Therefore, in the Board's judgement, the claims satisfy the requirement of clarity pursuant to Article 84 EPC.

2.3 Novelty

2.3.1 The random-access memory device known from document D1 (see in particular Figures 2A to 2I) is fabricated on a single semiconductor substrate (14) of a first conductivity type and comprises, in the terminology employed in claim 1:

a) a plurality of memory cells; and

b) at least one component field-effect transistor forming a part of a peripheral circuit;

in which each of said plurality of memory cells comprises:

a-1) a transfer field-effect transistor having first and second lightly-doped impurity regions (18a, 18b) of a second conductivity type opposite to said first conductivity type spaced apart from each other by a first channel-forming region, a first gate insulating film formed on said first channel-forming region, and a first gate structure (12) formed on said first gate insulating film,

a-2) a first inter-level insulating film (34) covering said first gate structure and exposing said first and second impurity regions (18a, 18b), and

a-3) a stacked-type storage capacitor having a lower electrode (20) formed on said first inter-level insulating film, a dielectric film structure (21) covering said lower electrode, and an upper electrode (22) held in contact with said dielectric film structure;

in which said at least one component field-effect transistor comprises:

b-1) third and fourth impurity regions of said second conductivity type spaced apart from each other by a second channel-forming region, each of said third and fourth impurity regions being implemented by a lightly-doped impurity sub-region (31) partially overlapped with a heavily-doped impurity sub-region (33),

b-2) a second gate insulating film formed on said second channel-forming region, and

b-3) a second gate structure (28) formed on said second gate insulating film and having side walls on side surfaces thereof, said side walls being made from an insulating film used for said first inter-level insulating film (34);

and said random-access memory device further comprising:

c) an upper inter-level insulating film structure (40) covering said plurality of memory cells and said at least one component field-effect transistor and having contact holes exposing said second impurity region and one of said third and fourth impurity regions, and

d) conductive wiring strips (41) passing through said contact holes and held in contact with said second impurity region and said one of said third and fourth impurity regions, respectively.

With regard to feature (a-3), the Board agrees with the appellant's submission that in the device of document D1 the stacked capacitor is held in contact with a highly-doped region, and is not in contact with the lightly-doped region, as required by the wording of claim 1.

Moreover, in the device known from document D1, each of said plurality of memory cells comprises a heavily-doped impurity sub-region having a dopant level corresponding to the heavily-doped impurity sub-region of the at least one component field-effect transistor, so that the known device does not comprise the feature (a-4) of the device of present claim 1.

2.3.2 Therefore, the subject-matter of present claim 1 is new over the prior art document D1 cited in the decision in the sense of Article 54 EPC.

2.4 *Inventive step - main request*

2.4.1 Claim 1

As set forth here above, the improvement over the RAM device known from document D1 comprises, in particular, in replacing the LDD-type field-effect transistors of the memory cells of this known RAM device by field-effect transistors with lightly-doped impurity regions only while leaving the at least one component field-effect transistor of the peripheral circuit unchanged.

Indeed, in the presently claimed RAM device, the component field-effect transistors of the peripheral part are of the LDD type, with lightly-doped and partially overlapping highly-doped impurity regions, as those in document D1.

The appellant's arguments (cf. item V) concerning the problem of loss of data bits in the RAM device known from document D1 and its solution by the present invention are convincing. In this connection, the problem of loss of data bits from the stacked capacitor is not mentioned in document D1. It could be argued that the skilled person would notice this problem during the routine operation of the known RAM device. However, in the Board's opinion, it would not be apparent to him that the loss of data bits was due to the provision of the highly doped region which is necessarily formed in the damaged area of the substrate. As the cause of the problem was not apparent from the cited prior art, its solution, i.e. the provision of a lightly-doped region without an overlap partly overlapping highly-doped region in contact with the stacked capacitor cannot be regarded as obvious to the person skilled in the art.

Therefore, in the Board's judgement, the subject-matter of present claim 1 involves an inventive step in the sense of Article 56 EPC.

Consequently, present claim 1 is patentable in the sense of Article 52(1) EPC.

2.4.2 Independent claim 5 relates to a process of fabricating a RAM device and specifies process steps which produce a device according to claim 1. In particular, the process step in feature (g) makes it clear that the

transfer field-effect transistor is not provided with a heavily-doped sub-region corresponding to the heavily-doped sub-region of the component field-effect transistor and that the stacked storage capacitor is held in contact with the highly-doped impurity region. The subject-matter of claim 5 therefore involves an inventive step for the same reasons as claim 1.

The dependent device claims 2 to 4 and process claims 6 to 11, which concern particular embodiments of the invention, are also patentable.

Therefore, a patent can be granted on the basis of the appellant's main request, so that it is not necessary to take into consideration the appellant's subsidiary requests (Article 97(2) EPC).

The description requires amendments for consistency with the subject-matter of the claims of the main request.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the claims 1 to 11 of the main request filed during the oral proceedings of 2 December 1999, and the description to be adapted to the claims.

The Registrar: The Chairman:

D. Spigarelli R. Shukla