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D E C I S I O N
of 22 February 2000

Case Number: T 0897/95 - 3.4.3

Application Number: 91201066.7

Publication Number: 0456318

IPC: H01L21/82

Language of the proceedings: EN

Title of invention:
CMOS process utilizing disposable silicon nitride spacers for making lightly doped drain transistors

Applicant:
Koninklijke Philips Electronics N.V.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - (yes)"

Decisions cited:
-

Catchword:
"In the examination of inventive step independent consideration in isolation of each of the plurality of the

features distinguishing the claimed subject-matter from the closest prior art is not correct, when the distinguishing features are interrelated."

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0897/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 22 February 2000

Appellant: Koninklijke Philips Electronics N.V.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 16 August 1995 refusing European patent application No. 91 201 066.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
A. C. G. Lindqvist

Summary of Facts and Submissions

I. European patent application No. 91 201 066.7 (publication No. 0 456 318) was refused in a decision of the examining division, dated 16 August 1995, on the ground that the subject-matter of claims 1 and 2 lacked an inventive step having regard to the prior art

document D1 = EP-A-0 356 202.

Claims 1 and 2 forming the basis of the decision read as follows:

"1. A method of fabricating a CMOS device of the LDD type in a semiconductor wafer comprising the steps of

(a) forming polysilicon gates (26; 28) overlying first (10) and second (12) conductivity type semiconductor regions in said wafer (14),

(b) forming spacers (34, 38; 35, 39; 36, 40; 37, 41) along the sides of the gates by growing a layer of silicon oxide (30) on the gates and semiconductor regions, depositing a further layer of silicon nitride (32) on the silicon oxide layer and performing an anisotropic etching step,

(c) forming a mask (52, 50) comprising a first protective layer (52) and a second overlying resist layer (50) to cover the gate-spacer structures (28; 36, 40; 37, 41) overlying the regions (12) of one conductivity type (n) and portions of the regions (12) of said one conductivity type (n) in which source/drain regions are to be formed and to leave uncovered the

gate-spacer structures (26; 34, 38; 35, 39) overlying the regions (10) of the other conductivity type (p) and portions of the regions (10) of said other conductivity type (p) in which source/drain regions are to be formed,

(d) implanting exposed surface portions of the regions (10) of the other conductivity type (p) with dopant of said one conductivity type (n),

(f) removing the second overlying resist layer (50) from the mask (52, 50),

(g) removing, with the first protective layer (52) of the mask (52, 50) still in place, the further layer (34; 35) from the spacers (26) and

(h) performing a blanket implant of dopant of said one conductivity type (n)."

"2. Method as claimed in claim 1, characterized in that in step (c) the mask (52, 50) is formed having a first protective layer (52) of silicon dioxide or silicon oxynitride."

In the decision under appeal, the examining division took the following view:

The method of claim 1 differs from the method known from document D1 in that different materials for the layers forming the spacers are used. Furthermore, the mask comprises a first protective layer and a second overlying resist layer and the second overlying resist layer is removed prior to removing the further layer

from the spacers.

The first difference merely constitutes an alternative. For selective etching of the spacer, it is essential that the two layers forming the spacer are of different materials. This is the case in both the method as claimed and in document D1. Accordingly, the objective problem addressed by this feature may be seen as providing alternative spacer materials.

The effect of the second difference is that in subsequent processing, after removal of the second overlying resist layer of the mask, a mask formed by the first protective layer may be used. Accordingly, the objective problem to be solved by this feature may be seen as providing a mask structure compatible with later processing steps.

Since the effects of the above differences are fully independent from each other, in the consideration of inventive step, the two objective problems defined above can be treated independently of each other.

The formulation of the problems to be solved as such does not have an inventive merit. It would be readily apparent to the skilled person in the field of semiconductor technology that the use of alternatives for the spacers as well as for the masks may be desirable.

The solution proposed by the present application would be an obvious alternative to the skilled person in view of the fact that both materials are well known and already used in document D1 for forming spacers, and

that they are well adapted for this purpose.

The solution proposed to the second of the above problems consists in forming a mask comprising a first protective layer and a second overlying resist layer, whereby the second overlying resist layer is removed prior to removing the further layer from the spacers.

The use of a two-layered mask is well-known in the art, for instance in conventional "hard" masks, whereby the resist layer is used for transferring the pattern by conventional photolithography into the underlying layer of a different material which is selected to be of, for example, a heat- or etch-resistant material in accordance with the specific needs.

Accordingly, the skilled person would use such a two-layered mask comprising a protective layer with an overlying resist layer, in accordance with circumstances, as a matter of routine practice, without exercising inventive skills.

Furthermore, it would be obvious to him to remove the overlying resist layer of the mask prior to any further processing steps where the presence of the resist is no longer wanted.

Therefore, the subject-matter of claim 1 lacks an inventive step.

The additional feature of claim 2 relates to the selection of particular materials for the protective layer, which materials are well known and commonly used in this technical field and clearly suitable as

protective masking layers in view of their known properties. This selection is thus a matter of routine practice and does not involve an inventive step.

II. The applicant lodged an appeal against this decision on 18 September 1995. On the same day, the appeal fee was paid and the statement of the grounds of appeal was filed.

III. With his letter dated 20 December 1999, the appellant (applicant) filed a single new claim to meet objections of lack of clarity expressed by the Board of appeal. This claim reads as follows:

"1. A method of fabricating a CMOS device of the LDD type in a semiconductor wafer comprising the steps of

(a) forming polysilicon gates (26; 28) overlying first (10) and second (12) conductivity type semiconductor regions in said wafer (14),

(b) forming spacers (34, 38; 35, 39; 36, 40; 37, 41) along the sides of the gates by growing a layer of silicon oxide (30) on the gates and semiconductor regions, depositing a further layer of silicon nitride (32) on the silicon oxide layer and performing an anisotropic etching step,

(c) forming a mask (52, 50) comprising a first protective layer (52), which comprises silicon oxide or silicon oxynitride, and a second overlying resist layer (50) to cover the gate-spacer structures (28; 36, 40; 37, 41) overlying the regions (12) of one conductivity type (n) and portions of the regions (12) of said one

conductivity type (n) in which source/drain regions are to be formed and to leave uncovered the gate-spacer structures (26; 34, 38; 35, 39) overlying the regions (10) of the other conductivity type (p) and portions of the regions (10) of said other conductivity type (p) in which source/drain regions are to be formed,

(d) implanting exposed surface portions of the regions (10) of the other conductivity type (p) with dopant of said one conductivity type (n),

(e) removing the second overlying resist layer (50) from the mask (52, 50),

(f) removing, with the first protective layer (52) of the mask (52, 50) still in place, the further layer (34; 35) from the spacers (26) and

(g) performing a blanket implant of dopant of said one conductivity type (n)."

IV. The appellant requests that the decision under appeal be set aside and that a European patent be granted on the basis of the following application documents:

Description: Pages 1 to 13 as filed;

The single claim filed with the appellant's letter of 20 December 1999;

Drawings: Sheets 1/4 to 4/4 as filed.

The appellant has submitted the following arguments in support of his request:

In step (b) of the method of the present claim, spacers are formed along the sides of the gates by performing an anisotropic etch after growing a layer of silicon oxide on the gates and semiconductor regions and depositing a layer of silicon nitride on the silicon oxide layer.

In step (c), a mask (50, 52) is formed comprising a first protective layer (52) comprising silicon oxide or silicon oxynitride and a resist layer (50) is then deposited on the mask.

As a result of the choice of materials of the layers of the spacers and of the layers of the mask (50, 52), the claimed method can be carried out easily and in a self-aligned manner; in particular:

1. the mask (50, 52) can be made easily;

2. the mask (50, 52) can be used during n^+ - implantation;

3. the protective mask (52) can be formed easily;

4. the protective mask (52) can be used during removal of spacers;

5. the protective mask (52) can be used during n^- - implantation;

6. the protective mask (52) can be improved with an annealing step;

7. due to the protective mask (52), annealing steps

of n^+ and n^- implants can be decoupled.

The claimed method in particular uses selective etching and masking properties of a plurality of materials of the spacers and of the mask (50, 52) which, in combination, results in a smooth process. The argumentation in the decision under appeal whereby each of the features distinguishing the present method from the method known from document D1 is treated separately cannot be correct. These distinguishing features are interrelated and, together, achieve the above mentioned advantageous results.

Therefore, the subject-matter of the sole claim involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Allowability of the amendments*

2.1 The claim as amended is a combination of claims 1 to 6 as originally filed. In particular, the amendment of step (c) that the mask comprises a first protective layer comprising silicon dioxide or silicon oxynitride is derivable from original claim 3.

Moreover, according to the description in the application as filed:

- the first protective layer (52) is the remaining portion of the layer (44) (see page 7, lines 7 to

8) underlying the resist layer (50) and, for this underlying layer (44), a bilayer of oxide and amorphous layer can be used as an alternative to silicon oxide (see page 6, lines 16 to 24);

- and, a layer of oxide and polysilicon can be used for the same first protective layer (52) (see page 7, lines 23 to 26).

Thus, the amendment in step (c) of the claim is consistent with the above cited text according to which silicon oxide may be employed with another material such as an amorphous layer or polysilicon.

Therefore, the Board is satisfied that the present application meets the requirement of Article 123(2) EPC that a European patent may not be amended in such a way that it contains subject-matter extending beyond the content of the application as filed.

The subject-matter of the present sole claim does not form part of the state of the art and is thus new in the sense of Article 54 EPC.

3. The only issue in the present appeal is that of inventive step

3.1 A method of fabricating a CMOS device of the LDD type in a semiconductor wafer (2) is known from document D1 (see Figures 1 to 9 and the corresponding text) comprising the steps of

(a) forming polysilicon gates (12) overlying first (n) and second (p) conductivity type semiconductor

regions (4; 6) in said wafer (2) (cf. Figure 1);

(b) forming spacers (18) along the sides of the gates (12) by forming a layer of silicon nitride (14) on the gates (12) and semiconductor regions (4; 6), depositing a further layer of silicon oxide (16) on the silicon nitride layer (14) and performing an anisotropic etching step (Figures 2 and 3);

(c) forming a mask of a resist layer (20) to cover the gate-spacer structures (18) overlying the regions (4) of one conductivity type (n) and portions of the regions of said one conductivity type (n) in which source/drain regions are to be formed and to leave uncovered the gate-spacer structures (18) overlying the regions (6) of the other conductivity type (p) and portions of the regions of said other conductivity type (p) in which source/drain regions are to be formed (cf. Figure 4);

(d) implanting exposed surface portions of the regions of the other conductivity type (p) with dopant of said one conductivity type (n) (cf. Figure 4),

(g) removing, with the resist layer (20) of the mask (20) still in place, the further layer (16) from the spacers (18) (cf. Figure 5); and

(h) performing a blanket implant of dopant of said one conductivity type (n).

3.2 The method of the present claim differs from the method of document D1 in that

(i) the arrangement of the layers forming the spacers is reversed in comparison to that in document D1, i.e. according to the invention the spacers are formed of a silicon oxide layer on the sides of the gates and a further layer of silicon nitride on the silicon oxide layer;

(ii) the mask according to the invention comprises a first protective layer comprising silicon oxide or silicon oxynitride, and

(iii) the first protective layer, as against a photoresist as in document D1, is used as a mask during the removal of the further layer of silicon nitride from the exposed spacer and during the blanket implant of the dopant of one conductivity type.

3.3 In the decision under appeal, the distinguishing process features (i) and (iii) were considered as addressing different unrelated aspects of the invention, and as a result were examined independently of each other in the consideration of inventive step. In this connection, however, the Board agrees with the appellant that the specific arrangement of the layers forming the spacers as set out in feature (i) above, and the use of the protective layer as a mask (cf. features (ii) and (iii) above) comprising silicon oxide or silicon oxynitride results in the selective removal of the further layer of silicon nitride from the spacer. Thus, the process features (i), (ii) and (iii) are interrelated and cooperate with each other, and have to be considered in combination in the examination of inventive step. This combination of the process

features is clearly not derivable from the prior art document D1, and also cannot be regarded as a commonly known measure in the production of CMOS devices.

The further prior art documents cited in the European search report are less relevant.

3.4 Therefore, in the Board's judgement, the subject-matter of the only claim was not obvious to the skilled person in view of the state of the art and thus involves an inventive step in the sense of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following application documents:

Description: Pages 1 to 13 as filed;

Claim: filed with appellant's letter of 20 December 1999;

Drawings: Sheets 1/4 to 4/4 as filed.

The Registrar: The Chairman:

D. Spigarelli R. Shukla