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D E C I S I O N
of 9 February 2000

Case Number: T 0876/95 - 3.4.3

Application Number: 89107334.8

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IPC: H01L 23/52

Language of the proceedings: EN

Title of invention:
Customizable semiconductor devices

Applicant:
QUICK TECHNOLOGIES LTD.

Opponent:
-

Headword:
Customizable semiconductor devices/QUICK TECHNOLOGIES

Relevant legal provisions:
EPC Art. 56, 123(2)

Keyword:
"Inventive step (no) - no evidence establishing a technical
prejudice in the art"

Decisions cited:
-

Catchword:
-



Case Number: T 0876/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 9 February 2000

Appellant: QUICK TECHNOLOGIES LTD.
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 20 April 1995
refusing European patent application
No. 89 107 334.8 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
W. Moser

Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division, dated 20 April 1995, to refuse European patent application No. 89 107 334.8. The application was refused on the ground that a set of claims filed in response to previous objections contravened Article 123(2) EPC. The amended claims included combinations of features that were not taught by the application as filed. In particular, dependent claim 2 was considered to contain certain features taken in isolation which, in the application as filed, were disclosed and claimed only in combination with other features necessary for defining a useful device. In addition, claims 3 and 5 to 8, when dependent on claim 2, resulted in further combinations being claimed which went beyond the contents of the original application. With respect to method claims 9 to 12, in so far as they related to devices as claimed in claims 2, 3 and 5 to 8, neither the originally filed claims nor the description provided a basis for the claimed methods.

In its decision, the examining division also noted that claims 2 to 4 and 5 to 7 did not satisfy the requirements of Article 84 EPC. It was not clear, for example, whether or not different expressions used in claims 2 to 4 and claims 5 to 7, respectively, were meant to indicate different features. The examining division also took the view that, in so far as the claimed invention was based on the original disclosure and could be understood with the aid of the description, it failed to meet the requirements of Article 52(1) EPC because it did not involve an inventive step in the sense of Article 56 EPC.

II. The following prior art documents were considered in the decision under appeal:

D2: ELECTRO/86 AND MINI/MICRO NORTHEAST, 11, (1986),
CONFERENCE RECORD, Los Angeles, USA, pages 1 to 4
of 18/5

D3: US-A-4 197 555

III. The notice of appeal was filed on 31 May 1995 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 23 August 1995. Oral proceedings took place on 9 February 2000.

IV. At the oral proceedings, the appellant (applicant) requested that the decision under appeal should be set aside and that a patent should be granted on the basis of:

(a) claims 1 to 7 filed on 23 August 1995 as main request, or

(b) claims 1 to 6 filed as auxiliary request during the oral proceedings.

V. Claim 1 of the main request reads as follows:

"1. A selectably customizable semiconductor device comprising:

(a) a first metal layer (74) disposed in a first plane and comprising first elongate strips (76, 150) extending parallel to a first axis;

(b) a second metal layer (70) disposed over said first metal layer (74) in a second plane generally parallel to and electrically insulated from said first plane and comprising second elongate strips (72, 152) extending parallel to a second axis, said second axis being generally perpendicular to said first axis, whereby a multiplicity of elongate strip locations (78) are defined at which the elongate strips (72, 76; 150, 152) of said first and second metal layers (70, 74) overlap in electrical insulating relationship;

(c) first layer fusible links (90) formed on said first layer (74), and

(d) second layer fusible links (82, 84, 102, 160, 172) formed on said second metal layer (70), said second layer fusible links (82, 84, 102, 160, 172) being formed as overlap fusible links (82, 84, 102, 160, 172) at locations which overlap said first elongate strips (76, 150)."

Claim 2 of the main request has the following wording:

"2. A selectably customizable semiconductor device according to claim 1, characterized in that:

said second metal layer (70) comprises a plurality of fusible conductive bridges (80) joining adjacent pairs of said elongate strips (72), said fusible conductive bridges comprising two of said overlap fusible links (82, 84) and including an electrical connection (88) formed between said first and second metal layers at a branch overlap location (88) disposed along said fusible conductive bridges between said two overlap fusible links, said electrical connection

joining said fusible conductive bridge to a particular one of the first elongate strips; and

including a fusible link (90) formed on said particular one of the first elongate strips and disposed adjacent to said two overlap fusible links."

VI. Claim 1 of the auxiliary request reads as follows:

"1. A selectably customizable semiconductor device comprising:

(a) a first metal layer (74) disposed in a first plane and comprising first elongate strips (76, 150) extending parallel to a first axis;

(b) a second metal layer (70) disposed over said first metal layer (74) in a second plane generally parallel to and electrically insulated from said first plane and comprising second elongate strips (72, 152) extending parallel to a second axis, said second axis being generally perpendicular to said first axis, whereby a multiplicity of elongate strip locations (78) are defined at which the elongate strips (72, 76; 150, 152) of said first and second metal layers (70, 74) overlap in electrical insulating relationship;

(c) first layer fusible links (90) formed on said first metal layer (74),

(d) electrical connections (88) being formed between said first metal layer (74) and second metal layer (70); and

(e) second layer fusible links (82, 84, 102, 160, 172) formed on said second metal layer (70), said second

layer fusible links (82, 84, 102, 160, 172) being formed as overlap fusible links (82, 84, 102, 160, 172) at locations which overlap said first elongate strips (76, 150), with some of said fusible links (82, 84) being formed between said second elongated strips (72) and said electrical connections (86, 88)."

VII. The arguments submitted by the appellant with respect to the main and auxiliary requests can be summarized as follows:

The amended claims 1 to 7 of the main request meet all the objections raised by the examining division, including those of lack of clarity and added matter. In particular, the subject-matter originally in claim 5 has now been introduced into claim 2. The amended claim 2 therefore no longer encompasses added matter and at the same time provides a complete definition of the invention. Having met the objections to claim 2 in respect of new matter, the same objections made in respect of other claims owing to their dependence on claim 2 are also met.

Claim 1 of the auxiliary request now provides a complete definition of the invention containing all the essential elements of the invention, and is properly supported by the description.

The appellant argued essentially as follows for the presence of inventive step in claim 1 of the main request and in claim 1 of the auxiliary request:

- (a) The invention provides customizable semiconductor circuits, in which fusible links are provided in conductor tracks formed in both the upper and the

lower layer, in which the tracks in both the upper and the lower layer are metal and in which fusible links in the upper layer are located above tracks in the lower layer.

- (b) Cutting in an upper layer of metal any links which are located above tracks in the lower layer is a difficult process because of the risk of causing damage to the track underneath if the fusible link is cut with a laser.

- (c) Cutting links in the lower metal layer was not possible until the inventor found a method for doing so. The new method is disclosed in another patent application. The other application has an earlier priority date than the application in suit, but was not published before the priority date of the latter. Accordingly, at the priority date of the application in suit there was no known method of laser-cutting conductors in the lower layer if those conductors were made of metal, and therefore the structure as claimed could not itself be obvious.

- (d) Document D2 relates to a customizable semiconductor device in which both upper and lower layer tracks are cut by laser; however, while the tracks in the upper layer are metal, polysilicon is used for the tracks in the lower layer. Polysilicon is cut with a laser more easily than a metal, and can be cut with a relatively low power laser beam. The appellant supported this contention by citing another document by the same author, to be referred to as Document D2', which contains an explicit reference to the use of

polysilicon tracks in the lower layer.

- (e) Document D3 discloses a structure in which the conductors in both the upper and the lower layer are metal. The document refers to two methods of cutting the links, laser light and chemical etching. All cuttable links are located in the upper layer.

Laser cutting would be unsuitable for fusing links in the lower layer because the comparatively high laser power required was likely to lead to damage in adjoining regions of the device.

Chemical etching would be unsuitable for cutting links because of difficulties in etching the same metal twice. Cutting links in the lower layer by chemical etching would also require further processing steps such as etching the insulating layer interposed between the metal conductors at the upper layer and the lower layer.

- (f) Documents D2 and D3 relate to different device structures and methods of cutting links. It is therefore not appropriate to combine the two documents in order to arrive at a finding that the device structure of the application in suit lacks an inventive step.

Reasons for the Decision

1. The appeal is admissible.

Main Request

2. *Amendments (Article 123(2) EPC)*

Claim 2 has been amended to meet the objection under Article 123(2) EPC which constituted the ground of refusal of the application in the decision under appeal. Claim 2 as amended combines the features claimed in the original claims 2 and 5. The original claim 5 relates to fusible links located in the second metal layer. Combining this feature which is an essential feature of the invention, with the features of claim 2 does not add new matter.

Claim 1 corresponds to claim 9 as originally filed, the originally filed independent device claims 1, 3, and 6, and their dependent claims 4, 5, 7, 8 and 10 to 13, have been cancelled, and method claims 14 to 17 as originally filed have been renumbered as claims 4 to 7.

Since the amendments to the claims do not add any matter which goes beyond the content of the application as filed, they are admissible under Article 123(2) EPC.

3. *Inventive step (Article 56 EPC)*

3.1 Document D2 is the closest prior art. The devices it relates to are laser-programmed semiconductor gate arrays. The devices consist of "...gate array chips with all elements connected by means of a universal network and a means of disconnecting the network at prescribed points in order to create a custom logic circuit." (page 1, second paragraph)

In particular, the network of conductors consists of a lower layer of largely parallel tracks, and an upper layer of largely parallel tracks orientated at right

angles to and insulated from the tracks in the lower layer. The network further includes diagonally extending link tracks, formed in the lower layer between pairs of parallel tracks. The link tracks serve to connect the parallel tracks in the lower layer to the parallel tracks in the upper layer. The connection is provided by vertical vias at locations which, when viewed from above, are the points of intersection between the diagonal tracks and the parallel tracks in the upper layer. Furthermore, tracks in both layers, that is to say, the parallel tracks in the upper layer and the parallel tracks in the lower layer, are provided with fusible links, as are the link tracks which provide the electrical connection between these two layers (cf. Figure 5 of document D2).

3.2 The device structure claimed in claim 1 of the main request differs from the structure known from document D2 in that the claimed structure includes "overlap fusible links" (claim 1, last paragraph). Overlap fusible links are fusible links which are formed in tracks of the upper layer at locations lying above tracks in the lower layer.

3.3 The appellant asserted that the tracks referred to in document D2 as being in the lower layer, are polysilicon tracks. This assertion about the contents of document D2 was supported with a reference to the related document D2' by the same author. Document D2', entitled "One day prototype laser programmed arrays", was allegedly submitted by Conrad J. Boisvert of Laserpath to an unnamed conference on 26 February 1986. The appellant did not provide any other evidence, and document D2' itself does not contain any dates, nor does it indicate the name of the conference concerned.

The Board nevertheless accepts that the assertion concerning silicon tracks in the lower layer is made plausible by the contents of document D2'. Thus, another difference to the disclosure in document D2 lies in the claimed device structure employing metal tracks in both the upper and the lower layer.

In view of the contents of document D2 as the closest prior art, the objective problem to be solved is that of providing a selectively customizable semiconductor device which has a compact structure using two layers of metallisation (cf. also the application as published, column 4, lines 30 to 35). The invention achieves the compact structure by providing fusible links in the upper and lower metal layers, and by locating fusible links in the upper layer above conductors in the lower layer ("overlap fusible links").

- 3.4 Document D3 relates to a semiconductor device comprising conductor tracks (202) in the lower layer and, electrically insulated from those tracks, tracks (201) in the upper layer. The tracks are of metal and are connected by vertical vias (203). Fusible links (204) are provided in the tracks (201) in the upper layer at locations overlying the tracks (202) in the lower layer (see, for example, Figure 10). Methods for removing unwanted lines, limited to breaking the electrical continuity of tracks in the upper layer only, are stated to include laser beams and chemical etching with a mask (column 5, lines 43 to 46).
- 3.5 Starting with document D2, which discloses a customizable integrated circuit structure in which links are located in both the upper and the lower layer

and in the conductors connecting these two layers, the skilled person addressing the problem of increasing the compactness of the semiconductor integrated circuit structure disclosed there, is taught by document D3 that fusible links in a dual metal layer structure can be placed above tracks in the lower layer. The skilled person is also taught by document D3 that such fusible links can be cut with a laser or by chemical etching.

3.6 The appellant argued that the disclosures of documents D2 and D3 could not be combined because at the priority date of the application in suit there was no known method of laser-cutting conductors in the lower layer if those conductors were made of metal. The Board noted that document D3 offered a choice of techniques for cutting the fusible links, including chemical etching.

3.7 Concerning the use of chemical etching, the appellant submitted that attempts at chemically etching tracks in the lower layer would be difficult because the same metal layer would be etched twice, the first time when the tracks were defined by etching the metal layer deposited to form the tracks, and the second time when the tracks were cut. It was generally accepted in the industry that etching a surface twice led to problems on account of surface reactions. In the absence of an acceptable cutting technique, the skilled person would not, therefore, provide a fusible link in the lower metal layer.

The Board agrees with the appellant that it would be somewhat cumbersome and difficult to use the wet and dry chemical etching techniques generally known in the art at the priority date of the application in suit, for cutting the fusible links in the lower metal layer.

However, in the absence of any prior art evidence establishing a technical prejudice against such use, the Board does not accept the appellant's submission that the difficulties in etching the lower fusible link using the available techniques would have deterred the skilled person from combining the teaching of documents D2 and D3.

- 3.8 The Board accepts that the method of fusing links in the lower metal layer, which forms the subject of another patent application and which is referred to on page 27 of the patent application in suit, may have helped to produce the new layouts and metallisation structures of the kind specified in the claim. The structure as claimed in claim 1 of the main request, however, does not indicate any product features which would enable the fusing of links in the lower metal layer. Hence, whatever contribution the new method might be thought to have made to improving the practical implementation of the claimed invention, that contribution cannot be taken into consideration in assessing the inventive step of the claimed structure.
- 3.9 For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 of the main request does not involve an inventive step.

Auxiliary request

4. *Amendments (Article 123 EPC)*

- 4.1 Claim 1 of the auxiliary request contains all the features of claim 1 of the main request and, in addition, the following two features, with the last sub-paragraph having been re-numbered from (d) to (e):

a new paragraph (d), "*electrical connections (88) being formed between said first metal layer (74) and second metal layer (70); and*",

and

in paragraph (e), before the full stop ", with some of said fusible links (82, 84) being formed between said second elongated strips (72) and said electrical connections (86, 88)".

4.2 The selective routing provided by the invention requires electrical connections between the first and second metal layer. This feature is described in general terms on page 9, lines 2 to 4 of the description, for example.

4.3 The second amendment to claim 1 specifies particular locations for at least some of the fusible links. The presence of fusible links at such locations is described with reference to and shown in Figures 3, 7 and 8 of the drawings and, as such, is based on the originally filed description.

4.4 In addition, the dependent method claim 6 relating to the use of ion milling to fuse the fusible links has been cancelled.

4.5 Since the amendments to the claims pertaining to the auxiliary request do not add any matter going beyond the content of the application as filed, they are admissible under Article 123(2) EPC.

5. *Inventive Step (Article 56 EPC)*

5.1 The same invention is claimed in claim 1 of the main request and in claim 1 of the auxiliary request, except that the latter additionally specifies particular locations for at least some of the fusible links and the electrical connections between the first and second metal layers. The specified locations for fusible links are on the conducting strips which together with the electrical connections (86, 88) form part of the electrical connection between the conducting strips in the first and second layers. Such locations are, however, known from document D2 (cf. paragraphs 3.1 (ii) and 3.5). All arguments concerning the obviousness of claim 1 of the main request apply therefore with equal force to claim 1 of the auxiliary request.

5.2 For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 of the auxiliary request also does not involve an inventive step.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla