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D E C I S I O N
of 9 November 2000

Case Number: T 0872/95 - 3.4.3

Application Number: 92201605.0

Publication Number: 0518418

IPC: H01L 21/76

Language of the proceedings: EN

Title of invention:
Method of manufacturing a semiconductor device whereby field oxide regions are formed in a surface of a silicon body through oxidation

Applicant:
Koninklijke Philips Electronics N.V.

Opponent:
-

Headword:
Oxidation mask/PHILIPS

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"
"Formulation of the objective technical problem"

Decisions cited:
-

Catchword:
-

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Case Number: T 0872/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 9 November 2000

Appellant: Koninklijke Philips Electronics N.V.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 17 July 1995 refusing European patent application No. 92 201 605.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. B. Günzel

Summary of Facts and Submissions

I. European patent application No. 92 201 605.0 was refused in a decision of the examining division dated 17 July 1995. The ground for the refusal was that the subject matter of claims 1 to 6 as filed lacked an inventive step having regard to the prior art documents

D1: US-A-4 755 477; and

D2: EP-A-0 424 018.

II. The reasoning of the examining division in the decision under appeal can be summarized as follows:

Having regard to the method disclosed in document D1, which method corresponds to the pre-characterizing portion of claim 1, the technical problem addressed by the application in suit relates to preventing defect formation at the surface of a silicon substrate due to stress caused by silicon nitride, rather than to preventing defects in a gate oxide layer, as stated in the application as filed. The formulation of the technical problem is based on the fact that firstly claim 1 neither specifies a gate oxide layer nor defines the step of removing the nitride layer, and thus does not contain any features relating to gate oxide, and secondly that the problem of defects formed at the surface of the substrate is addressed in document D2 for the same type of three-layer mask with silicon nitride sidewall, as in the application in suit.

A skilled person following the teaching of document D1 and concerned with eliminating defects in silicon

substrate would take the teaching of document D2 into consideration, where it is proposed to provide a stress relieving layer of silicon oxide on the exposed surface of the silicon substrate in a window prior to the formation of the nitride sidewall layer, and would thereby arrive at the claimed method.

III. The appellant (applicant) lodged an appeal on 9 September 1995, paying the appeal fee and filing a statement of the grounds of appeal the same day. A new claim 1 was filed with the statement of the grounds. Oral proceedings were requested in the event that the Board intended to reject the appeal.

IV. In response to a communication annexed to summons to oral proceedings, the appellant filed with the letter dated 5 October 2000 a new claim 1 forming the basis of an auxiliary request.

V. At the oral proceedings held on 9 November 2000, the appellant requested that the decision under appeal be set aside and a patent be granted on the basis of one of the following requests:

Main request:

Claim 1 filed with the statement of the grounds of appeal dated 6 September 1995; Claims 2 to 6 as originally filed; Description and Figures as originally filed.

Auxiliary request:

Claim 1 filed with the letter dated 5 October 2000; Description and Figures as originally filed.

VI. Claim 1 in accordance with the main request reads as follows:

"1. A method of manufacturing a semiconductor device in which a surface of a silicon body is provided with an oxidation mask, field oxide regions are formed through oxidation, the oxidation mask is etched away and a layer of gate oxide on the regions of the silicon body between the field oxide regions is formed through oxidation, whereby the oxidation mask is formed in a layered structure provided on the surface and comprising a lower layer of silicon oxide, an intermediate layer of polycrystalline silicon and an upper layer of a material comprising silicon nitride, in that windows are etched into the upper layer, the intermediate layer is removed by etching within the windows and below an edge of the windows, a cavity being formed below said edge, after which material comprising silicon nitride is provided in the cavity, characterized in that the material comprising silicon nitride is provided in the cavity while the surface of the silicon body situated within the windows is covered by a layer of silicon oxide."

VII. Claim 1 according to the auxiliary request differs from that of the main request in that the characterizing part reads as follows:

"characterized in that the intermediate layer is selectively etched with respect to the lower layer of silicon oxide during the etching treatment for forming the cavity below said edge and in that the material comprising silicon nitride is provided in the cavity

while the surface of the silicon body situated within the windows is covered by the lower layer of silicon oxide."

VIII. The appellant presented essentially the following arguments in support of his requests:

(a) The technical problem addressed by the present invention does not relate to avoiding defects due to stress from a nitride layer, as the examining division alleges, but relates to the prevention of defects in a gate oxide which are due to nitride residues on the substrate. The insight in the cause of the problem, i.e. that it is difficult to completely remove the oxidation mask layer of nitride when it is directly on the silicon substrate, is not derivable from any of the cited prior art documents.

(b) Document D1 states that the nitride layer 64 is sufficiently thin so that no defects are produced in the substrate (cf. D1, column 3, lines 24 to 29; column 5, lines 56 to 65). The skilled person following the teaching of document D1 would therefore not encounter any problem with defects produced in the silicon substrate, and would not, contrary to the view held by the examining division, have any reason to modify the process described therein.

(c) Document D2 discloses two different embodiments, the first embodiment where the nitride sidewall layer 25 is in direct contact with the silicon substrate (cf. Figures 1 to 6), and a second embodiment where a stress-relieving oxide layer 51

is grown on the exposed silicon substrate prior to the deposition of the nitride sidewall 25 in order to provide additional protection against defects (cf. Figures 7 to 10). Thus, the teaching of document D2 is in conflict with the teaching of D1 where it is stated that no stress relieving layer is needed (cf. D1, column 3, lines 24 to 30). In view of this contradiction, it was not obvious for the skilled person to combine the teaching of document D2 with the method of document D1.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Inventive step, main request*

2.1 Document D1, which represents the closest prior art, discloses a method of manufacturing a semiconductor device where oxide isolation regions 82 are formed using an oxidation mask which comprises a lower layer 22 of silicon oxide, an intermediate layer 34 of polysilicon, and an upper layer 42 of silicon nitride (cf. D1, column 4, line 8 to column 5, line 13). Windows are etched during the formation of the oxidation mask exposing the silicon substrate, and the intermediate layer is etched within the windows and below the edge of the mask to provide a cavity (cf. Figures 3 and 4). A silicon nitride layer 64 is formed in the cavity, on the sidewall of the oxidation mask, as well as on a portion of the silicon substrate surface (cf. Figures 8 and 9). After the field oxide 82 has been grown, the oxidation mask is removed, and gate

oxide layers of MOS transistors are formed on the exposed surfaces of the silicon substrate 10 in the active device regions (cf. Figure 11; column 6, lines 29 to 38).

Thus, all features of the pre-characterizing part of claim 1 are known from document D1.

2.2 The method of claim 1 according to the main request thus differs from that of document D1 in that a layer comprising silicon nitride is formed in the cavity while the surface of the silicon substrate situated within the windows is covered by a layer of silicon oxide. As a result, the silicon nitride layer is not in direct contact with the silicon substrate surface as in the method disclosed in document D1, since in the method of document D1, the silicon nitride layer 64 is deposited on the exposed silicon substrate through the windows.

2.3 As discussed in the application as filed, the method of document D1 has the disadvantage that it is difficult to remove the nitride oxidation mask layer completely when it is in direct contact with the silicon substrate (cf. page 1, line 27 to page 2, line 7). The presence of residual nitride layer on the active device region is, according to the application in suit, detrimental to the subsequent growth of a good quality gate oxide layer. Thus, the Board agrees with the appellant that the problem addressed by the invention as claimed in the amended claim 1 relates to the prevention of defects in the gate oxide. In this connection, the appellant also argued that the technical problem formulated by the examining division in the decision under appeal, i.e. the problem of preventing the growth

of defects in the substrate, could not be considered as the objective technical problem, since document D1 teaches that the oxidation mask described therein does not cause any defects in the silicon substrate (cf. item VIII(b) above). The Board, however, does not agree with this submission since the application in suit is also concerned with minimizing both the number of defects caused by the oxidation mask and the extent of lateral oxidation under the mask, i.e. the "bird's beak". This is apparent from the fact that the particular three-layer oxidation mask used in the method of claim 1 is known in the art to cause less defects than the conventional two-layer nitride/oxide oxidation mask (cf. page 1, line 1 to page 2, line 3 of the application as filed; document D1, column 3, lines 24 to 29; document D2, column 1, line 47 to column 2, line 12).

2.4 Therefore, the Board finds that the objective technical problem addressed by the present application not only relates to the prevention of defects in the gate oxide formed in the active regions surrounded by field oxide, but also to the reduction of the defect density in the surface of substrate in the active regions and of the "bird's beak".

2.5 As is generally known in the art, and this was not disputed by the appellant, a silicon nitride layer disposed directly on a silicon substrate surface tends to cause defects and dislocations in the silicon substrate. Therefore, one or more pad layers are conventionally provided between the nitride layer and the substrate surface to reduce stress between the nitride layer and the substrate (cf. the application in suit, page 1, lines 14 to 19).

In the method of document D1, a silicon nitride sidewall 64 is in direct contact with the silicon substrate. This measure has the purpose of reducing the "bird's beak" to a minimum (cf. D1, column 3, lines 24 to 29; column 5, lines 45 to 50). According to document D1, it is however only possible to maintain the silicon substrate surface free from defects and dislocations when the nitride sidewall layer contacting the substrate is subject to the constraints of being very thin and having only a narrow portion contacting the substrate surface (cf. D1, column 5, lines 9 to 13 and 56 to 65).

2.6 Document D2 which discloses a method for forming field oxide regions using a three-layer oxidation mask of the same kind as that of document D1, confirms the teaching of document D1 that a silicon nitride sidewall layer 25 may directly contact the silicon substrate surface 11 (cf. column 3, line 51 to column 4, line 4; Figures 4 and 5). However, when additional protection against the creation of defects in the substrate 11 is required, document D2 teaches that an additional oxide layer 51 should be provided between the substrate and the nitride sidewall layer (cf. column 4, lines 49 to 55; Figures 7 and 8).

2.7 Thus, a skilled person using the method of document D1 and faced with the technical problems as stated under point 2.4 above would consider the teaching of document D2 to be relevant. The application of the teaching of document D2 to the method of document D1 would moreover lead to a further simplification of the manufacturing process, since as readily realized, the step of removing the lower oxide layer 20 outside the masked regions can be omitted (cf. D1, Figure 6; column 4,

lines 65 to 68). Therefore, no inventive skills would be required in order to implement the teaching of document D2 to the method of document D1.

As to the argument by the appellant that the teaching of document D2 is contrary to that of document D1, so that the skilled person would not combine the two documents (cf. item VIII(c) above), it follows from the above discussion that there is no contradiction between the two documents: The teaching of the first embodiment of document D2 is in full agreement with that of document D1, i.e. a direct contact between the silicon nitride sidewall layer and the silicon substrate surface may provide a satisfactory result. The second embodiment of document D2, on the other hand, provides an improved protection against defect formation in the substrate surface, thus without contradicting the teaching of the first embodiment.

2.8 For the foregoing reasons in the Board's judgement, the subject matter of claim 1 according to the main request does not involve an inventive step within the meaning of Article 56 EPC.

3. *Inventive step, auxiliary request*

With respect to the method of claim 1 according to the main request, the method of claim 1 according to the auxiliary request further specifies that the intermediate layer is selectively etched with respect to the lower layer of silicon oxide, so that the lower layer of silicon oxide remains on the surface of the silicon substrate in the windows when the material comprising silicon nitride is deposited on the sidewall of the cavity.

The skilled person implementing the teaching of document D2 in the method of document D1 is faced with two alternatives, i.e. of growing a further oxide layer after removal of the lower oxide layer 20, or keeping the lower oxide layer 20 intact. As already stated under point 2.7 above, the latter alternative would lead to a simplification of the method of document D1 and would for this reason alone be obvious to the skilled person.

Therefore, the Board comes to the conclusion that the subject matter of claim 1 according to the auxiliary request does not involve an inventive step within the meaning of Article 56 EPC.

4. Thus, the appellant's main and auxiliary requests do not meet the requirement of inventive step according to Articles 52(1) and 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

L. Martinuzzi R. K. Shukla