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**D E C I S I O N**  
**of 31 August 2000**

**Case Number:** T 0851/95 - 3.4.3

**Application Number:** 90121295.1

**Publication Number:** 0427226

**IPC:** H01L 23/485

**Language of the proceedings:** EN

**Title of invention:**

Wiring pattern of semiconductor integrated circuit device

**Applicant:**

KABUSHIKI KAISHA TOSHIBA

**Opponent:**

-

**Headword:**

Wiring pattern for integrated circuit device/KABUSHIKI KAISHA  
TOSHIBA

**Relevant legal provisions:**

EPC Art. 84, 123(2)

**Keyword:**

"Main request: no support in the description for the invention  
as claimed (Article 84)"

"Auxiliary request: clarity (yes) - functional definition of  
features"

"Inventive step (yes, after amendments)"

**Decisions cited:**

-

**Catchword:**

-





**Case Number:** T 0851/95 - 3.4.3

**D E C I S I O N**  
**of the Technical Board of Appeal 3.4.3**  
**of 31 August 2000**

**Appellant:** KABUSHIKI KAISHA TOSHIBA  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 24 May 1995  
refusing European patent application  
No. 90 121 295.1 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** E. Wolff  
A. C. G. Lindqvist

## Summary of Facts and Submissions

I. The appeal lies against the decision of the Examining Division, dated 24 May 1995, to refuse European patent application No. 90 121 295.1. The application was refused on the grounds that the subject-matter of claim 1 was unclear and did not meet the requirements of Article 84 EPC (main request and first auxiliary request) and that the subject-matter of claim 1 of the second and third auxiliary requests extended beyond the content of the application as filed, contrary to Article 123(2) EPC.

In its decision the Examining Division also expressed the view that even if the stated objection to the claims were overcome by amendments, any such amended claims would fail to satisfy the requirements of Article 52(1) EPC, as either lacking novelty or an inventive step (Article 56 EPC).

II. The following prior art documents were considered in the decision under appeal:

D1: US-A-4 381 215

D2: EP-A-0 166 344

D3: EP-A-0 289 274

III. The notice of appeal was filed on 24 July 1995 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 29 September 1995. Oral proceedings took place on 31 August 2000.

IV. At the oral proceedings the appellant (applicant) requested that the decision under appeal should be set aside and that a patent be granted on the basis of the following documents:

(a) Main request

**Claims:** 1 to 4 as filed on 24 July 2000;

**Description:** pages 1 and 3 as filed on 24 July 2000, pages 6, 7 and 7a as filed on 12 January 1995 and pages 2, 4, 5 and 8 as filed on 30 May 1994;

**Drawings:** Figures 1A, 1B, 2, 3A to 3C and 4 to 7 as originally filed; or

(b) Auxiliary request

**Claims:** 1 to 3 as filed during the oral proceedings;

**Description:** pages 1 and 3 as filed on 24 July 2000, pages 6 and 7a as filed on 12 January 1995, pages 2, 4, 5 and 8 as filed on 30 May 1994 and page 7 as filed during the oral proceedings;

**Drawings:** Figures 1A, 1B, 2, 3A to 3C and 4 to 7 as originally filed.

V. Claim 1 of the main request reads as follows:

"1. A method of forming a wiring pattern in a semiconductor integrated circuit device, said wiring

pattern having a connection portion (Q) located on a connection hole (22) and a wiring portion (P) extending from a wiring portion side of said connection portion (Q), comprising the steps of

- selecting the width of connection portion margins (C) between the periphery of said connection portion (Q) to be formed and the periphery of said hole (22) as required to accommodate misalignment of said connection portion with respect to the location of said hole which misalignment may occur at random when forming said connection portion; and

- forming said connection portion (Q) in and around said hole without filling said hole such that a notch (S) is formed in that portion of said connection portion (Q) which is located in the hole (22), and said wiring portion (P) extending from said hole (22);

**characterized in that**

- in the step of selecting the width of said connection portion margins the width of the margin (B) on the wiring portion side of said connection portion (Q) is selected larger than the width required for accommodating misalignment that has been selected for the remaining margins (C) of said connection portion (Q)."

VI. Claim 1 of the auxiliary request reads as follows:

"1. A method of forming a wiring pattern in a semiconductor integrated circuit device, said wiring pattern having a connection portion (Q) located on a connection hole (22) and a wiring portion (P) extending from a wiring portion side of said connection portion (Q), comprising the steps of

- selecting the width of connection portion margins (B, C) between the periphery of said connection portion

(Q) to be formed and the periphery of said hole (22) as required to accommodate misalignment of said connection portion with respect to the location of said hole which misalignment may occur at random when forming said connection portion; and

- forming said connection portion (Q) in and around said hole without filling said hole such that a notch (S) is formed in that portion of said connection portion (Q) which is located in the hole (22), and said wiring portion (P) extending from said hole (22);

**characterized in that**

- in the step of selecting the width of said connection portion margins the width of the margin (B) on the wiring portion side of said connection portion (Q) is selected larger than the width required for accommodating misalignment that has been selected for the remaining margins (C) of said connection portion (Q);

- the width of the margin (B) on the wiring portion side of said connection portion (Q) being selected larger by an amount such that when said misalignment in a direction opposite to the wiring portion side occurs, the electrical connection hole resistance will not increase with respect to the electrical connection hole resistance value when there is no misalignment."

Independent claim 3 of the auxiliary request reads as follows:

"3. A method of forming a wiring pattern in a semiconductor integrated circuit device, said wiring pattern having a connection portion (Q) located on a connection hole (22) and a wiring portion (P) having a tapered portion extending from a wiring portion side of said connection portion (Q), comprising the steps of

- selecting the width of connection portion margins (B, C) between the periphery of said connection portion (Q) to be formed and the periphery of said hole (22) as required to accommodate misalignment of said connection portion with respect to the location of said hole which misalignment may occur at random when forming said connection portion; and

- forming said connection portion (Q) in and around said hole without filling said hole such that a notch (S) is formed in that portion of said connection portion (Q) which is located in the hole (22), and said wiring portion (P) extending from said hole (22);

**wherein**

- in the step of selecting the width of said connection portion margins the shortest distance (B) between the periphery of said tapered portion of said wiring portion (P) and the periphery of said hole (22) is selected larger than the width required for accommodating misalignment that has been selected for the remaining margins (C) of said connection portion (Q);

- said shortest distance (B) being selected larger by an amount such that when said misalignment in a direction opposite to the wiring portion side occurs, the electrical connection hole resistance will not increase with respect to the electrical connection hole resistance value when there is no misalignment."

VII. The arguments submitted by the appellant with respect to the main and auxiliary requests can be summarized as follows:

The purpose of the invention is to provide a connection of a wiring layer in a semiconductor device to a lower layer, separated from the wiring layer by, for example,



an insulating layer. Such connections should be small, simple, and reliable. One of the difficulties encountered in forming such connections stems from their small size, of the order of micrometers or even fractions of micrometers. Another difficulty arises from random misalignments between the connection hole and the metallisation of the wiring layer during masking operations as illustrated by Figures 3A to 3C of the application.

The applicants identified problems of lack of reliability of devices as being caused by these random misalignments, as a result of which current densities in a connection can locally exceed permitted values. The reliability problems arise from the fact that these connections may work for a limited time, for example, during device testing, only to fail later during operation.

The invention provides a solution whereby small, simple and reliable electrical connections are formed by an appropriate choice of the margins by which the metallised area exceeds the size of the connection hole.

Claim 1 of the main request defines a method of forming a wiring pattern in a semiconductor integrated circuit device. The margin of the connection portion on the wiring portion side is chosen larger than the remaining margins which are only slightly larger than what is required to accommodate random misalignments.

Independent claims of the auxiliary request define the width of the margin (B) as being such that when random misalignment occurs in a direction opposite to the

wiring portion side, the resistance of the connection will remain substantially the same as the resistance in the absence of any misalignment.

The choice of margins as claimed also provides a distinction over the cited prior art documents D1 and D2.

Independent claim 4 of the main request and independent claim 3 of the auxiliary request are directed towards configurations of the wiring layer in which the connection portion surrounding the hole tapers down to the dimension of the adjoining wiring section.

Otherwise the same comments apply as to claims 1 of the main and auxiliary requests.

## **Reasons for the Decision**

1. The appeal is admissible.

### *Main request*

2. *Support in the description (Article 84 EPC)*

Claim 1 relates to a method of forming a wiring pattern in which the part of the wiring pattern surrounding the connection hole, referred to as the connection portion, is selected "to accommodate misalignment of said connection portion with respect to the location of said hole which misalignment may occur at random when forming said connection portion". The method is characterised in that the "width of the margin (B) on the wiring portion side of said connection portion (Q) is selected larger than the width required for

accommodating misalignment...".

As described in the application as filed, the object of the invention is "to provide a wiring pattern of a semiconductor integrated circuit device in which the connection hole resistance does not increase" even if there is a random misalignment, referred to in the application as matching deviation, between the connection hole and the wiring layer (see column 2, lines 13 to 19 of the published application).

The invention is based on the applicant having found that the effect on the contact hole resistance of a random misalignment between the connection portion and the connection hole is not the same in every direction for a contact where the connection hole is only partially filled so that in the connection hole a notch is formed in the wiring layer (column 1, lines 17 to 18). As explained in the application with reference to Figures 3A to 3C, if the margin provided to accommodate random misalignment is the same in all directions, a random misalignment in which the wiring portion is displaced towards the hole has the effect of increasing the contact resistance while a misalignment in any other direction has only little effect on the connection hole resistance. This increase in the contact resistance, according to the application, may lead to disconnection of the wiring at the notch due to heat emission or electromigration.

As claimed in claim 1 of the main request, the invention provides for the margin on the wiring portion side of the connection portion to be selected larger than the width selected for the remaining margins. It is, however, not stated in the claim by how much the

selected width of the margin on the wiring side has to be larger. For the invention to achieve the object stated in column 2, lines 13 to 19, that margin must, according to the description of the invention, be sufficiently large for a misalignment of the wiring layer in a direction opposite to the wiring portion or in other words of a misalignment which brings the wiring portion closer to the connection hole, not to increase the connection hole resistance. (see for example column 4, lines 19 to 24). The feature that the width is sufficient for the connection hole resistance not to increase is, therefore, an essential element required to achieve the only stated aim of the invention. The invention as claimed in claim 1 is thus not consistent with the invention as described in the application as filed, so that there is no support in the description for the subject-matter of claim 1. Claim 1 of the main request therefore does not comply with Article 84 EPC.

3. *Auxiliary request*

3.1 Claim 1 of the auxiliary request differs from claim 1 of the main request in that it additionally specifies that the width of the margin (B, C) is "selected larger by an amount such that when said misalignment in a direction opposite to the wiring portion side occurs, the electrical connection hole resistance will not increase with respect to the electrically connection hole resistance value when there is no misalignment". This functional definition of the width of the margin (B) is clear since the electrical resistance of the connection hole can be readily determined by routine experiments.

The Board therefore concludes that claim 1 of the auxiliary request satisfies the requirements of Article 84 EPC.

Claim 3 of the auxiliary request is directed to wiring patterns in which the connection portion includes a tapered portion through which it is connected to the wiring portion of the wiring pattern. Except for a different definition for the margin (B), necessitated by the different geometry of this arrangement, the claim is identical to claim 1, making the discussion and the conclusion that the claim complies with the requirements of Article 84 EPC, equally applicable to this claim.

### 3.2 Amendments (Article 123(2) EPC

Claim 1 of the auxiliary request differs from any of the independent claims as originally filed in that the claim is directed to a method of forming a wiring pattern, while the claims as originally filled were directed to a wiring pattern as such. It is however, clear from the application as a whole that the invention lies in a method of forming a wiring pattern, with the special feature that the margins between the periphery of the hole and the connection portion are chosen as claimed.

The specific way in which, in accordance with the invention, the widths of the margins of the connection portion are determined, is explained on page 4, line 28 to page 5, line 3. The feature that the margin on the wiring portion side of the connecting portion is chosen such that the connection hole resistance is not increased even in the case where the wiring layer is

misaligned in the direction opposite to the wiring portion, is found on page 5, line 36 to page 6, line 6 and in Figure 5 of the drawings.

The Board therefore concludes that claim 1 of the auxiliary request complies with the requirements of Article 123(2) EPC.

Claim 3, the independent claim to configuration in which the connection portion is tapered towards the wiring portion, contains the further feature as compared to claim 1 that the geometry of the taper requires a different definition of the distance (B) between the periphery of the tapered portion and the periphery of the hole. It is clear from Figure 6 that the distance (B) is in fact the shortest distance between the periphery of the hole and the periphery of the tapered portion, thus supporting the definition of the distance (B) as being the shortest distance.

Claim 3 of the auxiliary request is otherwise the same as claim 1, the discussion and conclusion that the claim complies with the requirements of Article 123(2) EPC applies equally to this claim.

### 3.3 Inventive step

3.3.1 Document D2 concerns a contact structure for an emitter contact, the contact being made by filling a contact hole overlying the semiconductor structure with the metal of the wiring pattern. As shown in Figures 1A and 1B, the margin of the metallisation around the contact hole is not the same on all sides; instead, the margin extends further on what, in claim 1 of the application in suit is called the wiring portion, compared to the

other three sides around the contact hole where the margin is considerably narrower. In document D2, the margin on the wiring portion side is larger in order to extend from the emitter contact to a dielectric barrier. The barrier which takes the form of an insulating bump and the wide emitter contact extending to the barrier together serve to alleviate device degradation occurring as a result of electromigration-induced emitter stress. The larger margin around the hole in the direction of the barrier is thus determined by the spacing between the emitter contact and the dielectric barrier.

Document D1 also concerns a contact arrangement for a wiring pattern. In the description of the prior art in document D1, a wiring arrangement is illustrated in which a hole in an insulating layer covering a semiconductor structure is filled with metal. Using the language of claim 1 of the application in suit, the connecting portion is shown as being wider than the wiring portion by an amount which ensures that the whole area covered by the hole is completely filled with metal (column 1, lines 40 to 48). It is further explained that making the connection portion no wider than the wiring portion would lead to problems owing to misalignment tolerances which can cause the conductors to be off-set from the holes (column 1, lines 60 to 66). The potential consequences of such misalignment are explained, and it is stated that, if not for the extra widths of the margins, the number of interconnections made in a given area could be increased (column 1, lines 56 to 59). The solution proposed in document D1 involves the use of wiring patterns which are not widened in the area where contact is made. Instead a multilayer structure for the

contact area provides a protective layer over those areas which, through misalignment, are not covered by the wiring pattern.

- 3.3.2 Document D2 represents the closest prior art on account of the apparent similarity in the structure of the connection portion of the wiring pattern. Starting from document D2, the objective problem solved by the claimed invention is to find a configuration of the wiring pattern such that misalignments of the connection portion of the wiring pattern in relation to the contact hole do not lead to changes in the connection hole resistance, even though the metallisation of the connection hole is notched rather than completely filling the connection hole.

Neither document D2, nor document D1 deal with the case where the connection hole is not completely filled with metal. When the connection hole is completely filled with metal, a misalignment would generally not lead to connections in which a misalignment causes an increase in resistance which, in turn, could lead to those connections becoming defective in operation. Moreover, neither of the documents contains any information which would lead the skilled person to adopt a structure in which the margins are not only selected to be of a width sufficient to accommodate random misalignments between the wiring pattern and connection hole, but also to be sufficiently wide on the wiring portion side to fulfil the conditions stated in the last paragraph in claim 1. Concerning the apparent structural similarity between the contact arrangement disclosed in document D2 and that claimed in claim 1 of the application in suit, the Board observes that the extended margin on the wiring portion side in



document D2 is merely a function of the distance by which the barrier is spaced from the emitter contact. The purpose of the wider margins on one side of the connection hole is thus completely different from the purpose of the wider margin in the claimed invention.

In document D1, the only margins shown around the connection hole filled with metal are margins which are of the same width on all sides of the hole (Figure 1B and column 1, lines 46 to 48). Moreover, the solution adopted to solve the problem of misalignment between the connection hole and the wiring pattern does not involve any judicious choice of margin. Instead, it relies on a multilayer structure which protects those areas of a connection hole which through misalignment is not covered by the metal of the wiring pattern.

Neither document D2 nor document D1 consider the effect of random misalignments on the connection hole resistance of a notched connection hole. Given that the extended margin in document D2 serves a quite different purpose from the extended margin of the invention claimed in claim 1, in the Board's judgement the invention in claim 1 is not obvious over the cited prior art and involves an inventive step in accordance with Article 56 EPC.

The method of forming a wiring pattern as claimed in claim 3 differs from the method of claim 1 merely in that, owing to the tapered transition between the connection portion and the wiring portion a different definition for the margin (B) was required.

Accordingly in the Board's judgement the subject-matter of claim 3 of the auxiliary request also involves an

inventive step as required by Article 56 EPC.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent on the basis of the documents forming the auxiliary request.

The Registrar:

The Chairman:

L. Martinuzzi

R. Shukla