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D E C I S I O N
of 6 March 2002

Case Number: T 0734/95 - 3.4.3

Application Number: 90307848.3

Publication Number: 0410635

IPC: H01L 21/302

Language of the proceedings: EN

Title of invention:
Window taper-etching method in the manufacture of integrated circuit semiconductor devices

Applicant:
AT&T Corp.

Opponent:
-

Headword:
Etching mask/AT&T

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
"Inventive step (yes) - after amendment"
"Objecttive technical problem same as that stated in the application in suit"
"Closest prior art cited in the decision under appeal - not relevant for solving the technical problem addressed in the application in suit"

Decisions cited:
T 0881/92,

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0734/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 6 March 2002

Appellant: AT&T Corp.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 11 April 1995 refusing European patent application No. 90 307 848.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. B. Guenzel

Summary of Facts and Submissions

I. European patent application No. 90 307 848.3 was refused by a decision dated 11 April 1995 of the examining division on the ground that the subject matter of claims 1 to 12 filed with the letter dated 26 May 1994 did not involve an inventive step having regard to the prior art documents

D1: EP-A-0 127 946; and

D2: EP-A-0 030 116.

II. The reasoning in the decision for the finding of lack of inventive step can be summarized as follows:

Document D1 discloses a method of forming a tapered via hole in a dielectric comprising a first step of isotropic etching followed by a second step of anisotropic etching. The etching takes place in presence of a patterned photoresist layer formed on a patterned additional layer. The method of claim 1 differs from that of document D1 in that the patterned photoresist layer is left on the additional layer during the etching of the dielectric layer, whereas in document D1, it appears that the photoresist is removed after patterning the additional layer. It is however not explicitly specified in document D1 what happens to the photoresist.

The above differences are considered to be merely a matter of routine design practice for the following reasons: Since the additional layer serves as a dimensionally stable mask during the etching of the dielectric layer, the patterned photoresist may be

removed directly after the etching of the additional layer or may equally be left in place and removed only at a later stage. Which option the skilled person would choose is a matter of routine design practice in accordance with the circumstances. Since document D1 does not mention what happens to the photoresist and only shows the resulting structure after the etching of the dielectric is completed, the skilled person has to decide at which stage the photoresist should be removed. It is also regarded obvious to select the material of the additional layer such that the adhesion to both the dielectric layer and the photoresist is sufficient.

III. The appellant (applicant) lodged an appeal on 6 June 1995, paying the appeal fee on 2 June 1995. A statement of the grounds of appeal was filed on 10 August 1995.

IV. In response to communications of the Board and a telephone consultation dated 22 November 2001, the appellant filed new application documents with the letters dated 18 August 2000 and 4 December 2001.

The appellant requests that the decision under appeal be set aside and a patent be granted based on the following documents:

Claims: 1 filed with the letter dated 4 December 2001
2 to 7 filed with the letter dated 18 August 2000
8 to 12 filed with the letter dated 26 May 1994

Description: Page 1 filed with the letter dated

18 August 2000
Pages 2 to 4 as originally filed

Drawings: Sheet 1/1 as originally filed.

Furthermore, oral proceedings are requested in the event the Board intends to dismiss the appeal.

V. Claim 1 according to the appellant's request reads as follows:

"1. A method for making an integrated circuit comprising the steps of:
making an opening in a dielectric (11), said opening being etched in the presence of a patterned photoresist layer (13), said photoresist layer (13) having a first opening with a first dimension; and

said etching comprising a first step of isotropic etching and followed by a second step of essentially anisotropic etching, both the first and second etching steps being carried out in the presence of the patterned photoresist layer (13), wherein the method further comprises the steps of:

prior to deposition of said photoresist layer (13), depositing an additional layer (12) on said dielectric (11), the material of said additional layer (12) being selected to enhance adhesion of photoresist layer (13) to the dielectric, said additional layer (12) being etched to create a second opening with a second dimension prior to said etching of said dielectric (11), said first and second dimensions

remaining substantially equal during both said isotropic and said anisotropic etching."

VI. The appellant presented essentially the following arguments in support of his request:

The claimed method relates to a different method from that of document D1: Claim 1 requires the use of two materials, a photoresist and an additional layer where the additional layer (i) must retain dimensionally stable during the etching, and (ii) must promote adhesion between the overlying photoresist and underlying dielectric layer. The use of a photoresist together with the underlying dimensionally stable adhesion promoter is not even remotely taught or suggested in document D1.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and clarity*

Claim 1 contains the feature of claim 1 as originally filed and further specifies that (i) the additional layer has an opening of substantially the same dimension as that of the photoresist; (ii) the patterned photoresist is present during both etching steps; and (iii) the additional layer is selected to enhance adhesion of photoresist layer to the dielectric. Features (i) to (iii) are disclosed on page 2, line 35 to page 3, line 3, Figure 4, and page 2, lines 21 to 25, respectively, of the application as filed. Claims 2 to 8 correspond,

respectively, to claims 2 to 8 as originally filed. The different alternatives in claims 9 and 10 as originally filed are now separately claimed in claims 9 to 12.

Therefore, in the Board's judgment, the requirements of Article 123(2) EPC are met. The Board furthermore considers the claims to be clear, as required by Article 84 EPC.

3. *Inventive step*

3.1 The application in suit relates to a process of forming a tapered via hole in a dielectric layer using a patterned photoresist layer as an etching mask. The prior art method described in the application in suit comprises an isotropic etching step followed by an anisotropic etching step. The problem with the above prior art method is that the photoresist layer used to define the via hole has a tendency to peel off during this process, due to the fact that a portion of the dielectric layer below the edge of the photoresist is removed during the isotropic etching step, a phenomenon known in the art as "undercutting".

As a solution to the above problem, the method according to claim 1 specifies that an intermediate layer is formed between the dielectric and the photoresist which serves as an adhesive between the photoresist and the dielectric layer. The intermediate layer and the photoresist both remain unaffected by the etching process insofar that the dimensions of the openings in the intermediate layer and the photoresist remain substantial equal during both etching steps.

3.2 Document D1, which was considered the closest prior art

in the examination procedure, discloses a method of producing a tapered via hole in a dielectric 8 made of polyimide. The method comprises an isotropic etching step followed by an anisotropic etching step (cf. Figure 2; page 5, line 11 to page 6, line 15). The etching mask is formed of a patterned layer 9 made of a non-erodable material, such as titanium (cf. page 5, lines 22 to 24 and 28 to 30) which is patterned using "conventional photolithography", ie the opening 10 is formed using a photoresist as a mask (cf. D1, page 5, lines 24 to 25). It follows from the description on page 5, lines 27 to 30 that after the formation of the opening 10, the mask layer is used as an etching mask during the subsequent etching of the via in the dielectric layer. Thus, it does not follow from the description that the photoresist used to form the opening 10 is used as an etching mask during the etching of the via in the dielectric. Also, it follows from Figure 2 that the photoresist is used only to pattern the etching mask 9.

3.3 The method of claim 1 differs from that of document D1 in that the patterned photoresist layer is present during the etching of the dielectric layer. Furthermore, the method of claim 1 specifies that the material of the additional layer is selected to enhance adhesion of the photoresist layer to the dielectric.

3.4 As mentioned under item 3.1 above, the application in suit relates to a method of forming a tapered via hole in a dielectric layer where a photoresist layer is used as etching mask in an isotropic etching step followed by an anisotropic etching step. The technical problem addressed by the application is suit relates to preventing the photoresist layer from peeling off the

dielectric layer (cf. application as filed, page 1, lines 22 to 31).

3.4.1 In the method of document D1, on the other hand, the above problem does not occur, since it does not relate to the use of a photoresist as an etching mask for the dielectric layer. The dielectric layer in document D1 is a polyimide layer. As mentioned in US-A-4 495 220, which was cited in the official search report of the application in suit, polyimide has the property that it is etched at about the same etching rate as conventional photoresist materials (cf. column 1, lines 54 to 66). Therefore, the mask layer 9 made of titanium acts as etching mask in the method of document D1. The photoresist layer used for defining the opening in the additional layer is automatically removed in the course of the isotropic and anisotropic etching steps due to the similar etching properties of polyimide and photoresist.

3.5 Document D2 discloses a method of patterning and etching a polycrystalline silicon layer 13 into wiring layers. Using a photoresist layer 15 as a mask, the polycrystalline silicon layer 13 is subject to an isotropic etching step followed by an anisotropic etching step (cf. Figures 6 to 9 with accompanying text). The method produces wiring layers with tapered sidewalls which facilitates the deposition of a uniformly thick insulating layer 14 on the wiring layers.

Thus, in contrast to the claimed method, the method of document D2 is not concerned with forming tapered via holes in a dielectric layer.

3.6 The boards of appeal have held on more than one occasion that an objective definition of the technical problem to be solved should normally start from the technical problem actually described by the applicant, unless it turns out that an incorrect state of the art was used to define the technical problem or that the technical problem disclosed has in fact not been solved (see T 0881/92, cited in "Case Law of the Boards of Appeal, 3rd Edition", Section I.D.4.1). In the present case, the Board finds that none of the documents D1 and D2 form a prior art closer than that acknowledged in the application in suit, since document D1 discloses a method where a photoresist would not be suitable as an etching mask, and document D2 is not concerned with the formation of tapered via holes in a dielectric. Moreover, the Board does not have any doubts that the technical problem described in the application is solved by the claimed method.

Therefore, the objective technical problem addressed by the application in suit is the same as that described in the application in suit, ie preventing an etching mask made of photoresist from peeling off a dielectric layer in a process where the dielectric layer is subject to an isotropic etching step followed by an anisotropic etching step (cf. items 3.1 and 3.5 above).

3.7 In the light of the above considerations, a skilled person concerned with the technical problem addressed by the application in suit, would not consider document D1 to be relevant.

Consequently, in the Board's view it was not a matter of mere design practice, as held in the decision under appeal, to decide whether the photoresist layer used

for forming the opening in the mask layer 9 in the method of document D1 is kept during the course of etching the polyimide layer or not, since the photoresist layer is etched at about the same rate as polyimide, and is thus automatically removed in the course of forming the tapered via hole.

Since document D2 is not concerned with the etching of tapered via hole in a dielectric layer, the teaching of document D2 is not relevant for the technical problem addressed by the application in suit.

Therefore, in the Board's judgement, the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents according to the appellant's request as specified under item IV above.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla