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D E C I S I O N
of 23 May 2000

Case Number: T 0625/95 - 3.4.3

Application Number: 88111617.2

Publication Number: 0300433

IPC: H01L 21/18

Language of the proceedings: EN

Title of invention:
Method for manufacturing bonded semiconductor body

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2), 56

Keyword:
"Inventive step - (yes) auxiliary request"
"Amendement - removal of a feature (not allowed)"

Decisions cited:
T 0331/87

Catchword:
-

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Case Number: T 0625/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 23 May 2000

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 13 February 1995 refusing European patent application No. 88 111 617.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 88 111 617.2 was refused in a decision of the examining division dated 13 February 1995. The ground for the refusal was that the subject matter of claims 1 to 6 lacked an inventive step with respect to the prior art documents

D1: EP-A-0 190 935; and

D2: Patent Abstracts of Japan, vol. 11, No. 341 (E-554) 7 November 1987 & JP-A-62 122 141.

II. The appellant (applicant) lodged an appeal on 13 April 1995, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 22 June 1995 together with new claims 1 to 7 and an amended description. Additionally, oral proceedings were requested in case the Board intended to dismiss the appeal.

III. In a communication annexed to a summons to oral proceedings, the Board informed the appellant of its provisional opinion that the subject matter of claim 1 did not seem to meet the requirements of Articles 123(2), 84 and 56 EPC. The Board furthermore introduced the following prior art document cited in the European search report into the appeals proceedings:

D3: EP-A-0 190 508.

IV. With his letter dated 25 April 2000, the appellant filed new claims 1 to 5 as a first auxiliary request, the claims filed with the statement of the grounds of

appeal forming a main request.

V. At the oral proceedings held on 23 May 2000, the appellant submitted a copy of the Japanese Industrial Standard JIS B 0601 (1994) and filed a new set of claims 1 to 5 together with an amended description forming a first auxiliary request. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the claims according to one of the following requests:

Main request:

Claims: Nos. 1 to 7 filed with the statement of the grounds of appeal on 22 June 1995;

Description: Pages 4, 4a, 9, and 10 as filed with the statement of the grounds of appeal on 22 June 1995;
Pages 1 to 3, 5 to 8, and 11 as originally filed

Drawings: Sheets 1/5 to 5/5 as originally filed

Auxiliary request:

Claims: Nos. 1 to 5 (auxiliary request) as filed during the oral proceedings on 23 May 2000

Description: Pages 4, 4a, 9, and 10 as filed with the statement of the grounds of appeal on 22 June 1995;
Pages 1 to 3, 5 to 8, as originally filed;
Page 11 as filed during the oral proceedings on 23 May 2000

Drawings: Sheets 1/5 to 5/5 as originally filed.

VI. Claim 1 in accordance with the main request reads as follows:

"1. A method of manufacturing a bonded semiconductor body, comprising the steps of:

(a) preparing semiconductor substrates (1,2) each having a flat mirror surface with a surface roughness less than 130 Å;

(b) bringing the flat mirror surfaces of first and second semiconductor substrates (1,2) together in close contact in pairs at a bonding interface (3) of each pair, to provide the bonded semiconductor body;

(c) subjecting the bonded semiconductor body to infrared topography to detect images corresponding to voids on the bonding interface of said first and second semiconductor substrates (1,2); and

(d) selecting particular bonded semiconductor bodies in which no image like a Mars pattern appears."

VII. Claim 1 in accordance with the auxiliary request reads as follows:

"1. A method of manufacturing a bonded semiconductor body, comprising the steps of:

a) preparing a first semiconductor substrate (1) with a flat mirror surface;

b) preparing a second semiconductor substrate (2) with a flat mirror surface;

c) bringing the mirror surface of said first semiconductor substrate (1) into close contact with the mirror surface of said second semiconductor substrate (2) to form a

semiconductor body (4);

d) subjecting said semiconductor body (4) to a heat treatment at a temperature equal to or higher than 200° C and lower than the melting point of said first and second semiconductor substrates (1,2) for a given period of time in a predetermined atmosphere, whereby said bonded semiconductor body is formed;

characterized by:

e) providing said flat mirror surfaces of said first and second semiconductor substrates (1,2) with a surface roughness equal to or less than 13 nm (130 Å) in a range of 1 mm length;

f) observing said semiconductor body by use of infrared topography before said heat treating step for selecting those semiconductor bodies providing an image of uniform intensity, for said heat treatment."

Claims 2 to 5 of the auxiliary request are dependent on claim 1.

VIII. The appellant presented essentially the following arguments in support of his requests:

(a) Claim 1 according to the main request does not include a heat treating step, since this heat treatment is not seen as a key feature of the method according to the present invention.

(b) As to the auxiliary request, the step f) is based on the disclosure on page 4, lines 16 to 19, page 3, lines 3 to 16 and 19 to 23 where it is evident that the step of observing the semiconductor body by infrared topography has to be performed before the heat treating step. The

feature of claim 8 as filed where the above-mentioned step of observing by infrared topography is carried out *after* the heat treating step is erroneous, since it is in contradiction with the rest of the application as originally filed.

(c) Although infrared topography was a known method for detecting defects in bonded semiconductor bodies, such as described in document D2, this was only carried out after the step of heating the bonded wafers, in contrast to the claimed method where the step of observing the bonded interface using IRT is carried out *before* the heating step: The "Mars pattern" images were known to disappear after the heating step, whereas the patterns caused by dust particles trapped between the substrates would remain. Consequently, in the art of bonding semiconductor wafers, the significance of the "Mars patterns" was not recognized and they were regarded as spurious. It was therefore considered more convenient to carry out the IRT detection after the heating step, so as to detect dust particles.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Main request*

2.1 Amendments

Claim 1 as amended is based on claim 1 as filed,

however the step of heating the substrates in close contact with each other, as in claim 1 as filed, is omitted from the amended claim 1.

Following the principles set out in decision T 331/87 (OJ EPO 1991, 22), the removal of a feature in an independent claim may not violate Article 123(2) EPC provided that the skilled person directly and unambiguously recognizes that (1) the feature was not explained as essential in the disclosure, (2) it was not, as such, indispensable for the function of the invention in the light of the technical problem it serves to solve, and (3) the replacement or removal required no real modification of other features to compensate for the change (cf. also Guidelines, C-VI, 5.8a).

Although the heating step is not as such disclosed in the application in suit as essential, the application only concerns the improvement of the quality of a bond produced by (a) joining two mirror-polished wafers; and (b) heating the joined wafers. Having regard to this object of the invention, the Board has serious doubts whether the measures proposed in the application in suit (roughness less than 13 nm and absence of "Mars" patterns in the infrared topography image) would achieve this object without the presence of a heating step, since according to the application in suit, the heating step has the effect of increasing the bonding strength between two wafers from about 5 kg/cm^2 to about 100 kg/cm^2 (cf. page 2, lines 8 to 12). Thus, the increase in bonding strength obtained by using wafers having the claimed limit of roughness and by the selection of wafers using infrared topography alone do not compensate for the absence of a heating step. The

Board therefore finds that the criterion (3) is not met.

Therefore, in the Board's judgement, claim 1 of the main request does not meet the requirements of Article 123(2) EPC.

3. *Auxiliary request*

3.1 Amendments and clarity

3.1.1 Claim 1 according to the auxiliary request contains the features of originally filed claims 1 and 5, and the features disclosed on page 4, lines 29 to 34 (definition of surface roughness in step e)), page 4, lines 16 to 19, page 3, lines 3 to 16 and 19 to 23 (step f)). Claim 2 is based on the disclosure on page 11, lines 5 to 10, and claims 3 to 5 contain the features of claims 2, 6, and 7 as filed, respectively.

3.1.2 It is specified in step f) of claim 1 that the semiconductor body is observed using infrared topography (IRT) "before said heat treating step", whereas claim 8 as originally filed states that the observation using IRT is carried out *after said heat treatment.* The appellant argued that since claim 8 is in contradiction with the rest of the application as filed, it must be disregarded when assessing whether the requirements of Article 123(2) EPC are met.

The Board agrees with the submissions of the appellant, since claim 8 as filed has no support in the description as filed: The passages on page 3, lines 3 to 16 and 19 to 23 of the application as filed referring to the prior art states that it was known

that when bonded semiconductor bodies were observed by IRT, dark portions having a shape reminiscent of the surface of the moon or Mars may be observed (in the following referred to as "Mars pattern"), but that these dark portions disappear after suitable heat treatment. Moreover, in the description of the embodiments of the invention, no details are given when the observation by IRT is carried out. Thus, a skilled person reading the application in suit would infer firstly that it would make no sense to look for "Mars patterns" after the heat treatment, since such patterns would have disappeared, and secondly, since the description of the embodiments of the invention does not indicate any particular details how the observations by IRT is carried out, the reader skilled in the art would infer that this step should be carried out as previously described.

3.1.3 Therefore, in the Board's judgement, the requirements of Article 123(2) EPC are met. The Board furthermore consider the claims to be clear, as required by Article 84 EPC.

3.2 Inventive step

The only remaining issue in the appeal is that of inventive step.

3.2.1 Document D1 which is the closest prior art, discloses a method of bonding two semiconductor substrates (cf. D1, page 5, lines 1 to 25; Figures 1A to 1C). The method comprises the steps of selecting semiconductor substrates each having a flat mirror surface with a surface roughness less than 50 nm, bringing the polished surfaces of two semiconductor substrates (11,

13) together to form a semiconductor body; and subjecting the semiconductor body to a heat treatment at a temperature of 1000 to 1200° C.

3.2.2 Thus, the claimed method differs from that of document D1 in that (i) the surface roughness is less than or equal to 13 nm in a range of 1 mm length; and (ii) IRT is used before the heating step to select void-free semiconductor bodies. Document D1 on the other hand does not employ any techniques for controlling the quality of the bond between the two substrates. On the contrary, the device of document D1 has a highly doped layer 12 at the bond interface which allows the current to bypass a void at the interface without causing a major increase in the resistance of the current path (cf. D1, page 5, lines 31 to 37; Figure 1C).

3.2.3 The objective technical problem addressed by the present invention is thus to produce bonded semiconductor bodies having an improved bonding strength and increasing the yield of diced semiconductor chips.

As described in conjunction with Figures 1C and 1D of the application in suit, the above problem should in particular be considered under the circumstances where the bonded semiconductor body is diced into small chips containing a plurality of circuit elements. A single void in the interface may disrupt the current flow across the entire chip or cause the bonded chips to peel off.

3.2.4 It is common general knowledge in the art that the presence of voids at the interface between two bonded substrates affects the quality, i.e. the strength of

bonding, and that the number of voids at the interface is in turn influenced by the degree of roughness of the surfaces to be joined. For a skilled person, therefore, it would be obvious that a lower degree of roughness, i.e. lower or equal to 13 nm was likely to improve the bonding strength.

3.2.5 Document D2 describes a method, known as infrared topography (IRT), to detect the presence of voids at the interface of two wafers (1, 2) bonded to each other (cf. D2, abstract). The method is based on the realization that unbonded parts, i.e. voids at the interface, cause enhanced infrared reflection in relation to bonded parts free of voids. It is also clear from the content of the document D2, that the detection of the voids is carried out on a **bonded** structure.

3.2.6 In contrast to the use of IRT in the prior art, the claimed method uses IRT to detect voids due to surface roughness prior to the bonding of the surfaces.

It was argued by the appellant that the surface roughness of equal to or less than 13 nm over 1 mm of length as required in claim in suit, alone does not ensure that the **bonded** structure has a void free interface and consequently a high bonding strength, since the measured roughness is only over 1 mm length at selected locations on the substrate surface and not uniformly over the whole of the surface. Consequently, an additional step of ensuring a uniform surface roughness over the entire substrate surface is required before the substrates are heated to bind them together. Such a uniform surface roughness is ascertained in the claimed method by the absence of the so-called "Mars

pattern", i.e. when the IR image has a uniform intensity.

The Board finds that the above submissions are supported by the description in the application as filed on page 3, lines 3 to 24; page 4, line 35 to page 5, line 3, and page 5, line 33 to page 6, line 7. Also it follows from the above cited passages that in the art, the significance of the "Mars pattern" in the IR image prior to bonding was not realized, and that they were regarded as spurious as they disappeared after the bonding by heating.

Thus, the Board finds that there was no hint or suggestion in the prior art to use the method of document D2 prior to bonding as specified in claim 1 according to the auxiliary request.

3.2.7 Therefore, in the Board's judgment, the subject matter of claim 1 according to the auxiliary request involves an inventive step within the meaning of Article 56 EPC, and meets the requirements of Article 52(1) EPC. Dependent claims 2 to 5 also therefore comply with the requirement of Article 52(1) EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant the patent on the basis of the following:

Claims: Nos. 1 to 5 (auxiliary request) as filed during the oral proceedings on 23 May 2000

Description: Pages 4, 4a, 9, and 10 as filed with the statement of the grounds of appeal on 22 June 1995;
Pages 1 to 3, 5 to 8, as originally filed;
Page 11 as filed during the oral proceedings on 23 May 2000

Drawings: Sheets 1/5 to 5/5 as originally filed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla