BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen

D E C I S I O N
of 7 July 1999

Case Number: T 0546/95 - 3.4.3

Application Number: 88311837.4

Publication Number: 0323078

IPC: H01L 23/52

Language of the proceedings: EN

Title of invention:
Electrically-programmable low-impedance anti-fuse element

Applicant:
ACTEL CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 113(1), 123(2), 56
EPC R. 67

Keyword:
"Subject-matter extending beyond the content of the application as filed (no - after further amendments)"
"Inventive step (yes)"
"Procedural violation (no)"

Decisions cited:
T 0951/92

Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0546/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 7 July 1999

Appellant: ACTEL CORPORATION
955 East Arques Avenue
Sunnyvale
California 94086 (US)

Representative: Senior, Alan Murray
J. A. KEMP & CO.
14 south Square
Gray's Inn
London WC1R 5LX (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 16 January 1995 refusing European patent application No. 88 311 837.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
W. Moser

Summary of Facts and Submissions

I. European patent application No. 88 311 837.4 (publication No. 0 323 078) was refused in a decision of the Examining Division of 16 January 1995 on the grounds that the subject-matter of claim 1 lacked an inventive step having regard to **E1** = EP-A-0 250 078 and that the subject-matter of the independent claim 8 as amended extended beyond the content of the application as filed.

Claims 1 and 8 forming the basis of the decision under appeal read as follows:

"1. An electrically programmable, low-impedance antifuse element (13) disposed in an integrated circuit, including:

a first electrode (12a, b) comprising a region in the substrate (10) of said integrated circuit containing arsenic at a concentration of between about 1×10^{19} to 1×10^{22} atoms/cm^3, said region having an arsenic pileup doping profile;

a dielectric layer (14) disposed over said first electrode; and

a second electrode (22a, 22b) comprising a layer of arsenic-containing polysilicon disposed over said dielectric layer."

"8. An electrically-programmable, low-impedance antifuse element (36) disposed in an integrated circuit, including:

a first electrode (46) disposed on an insulating layer (42), said first electrode comprising a layer of arsenic-containing polysilicon, wherein the arsenic concentration of said first electrode has an arsenic pile up doping profile;

a dielectric layer (48) disposed over said first electrode;

a second electrode (50) comprising a layer of arsenic-containing polysilicon disposed over said dielectric layer."

II. In the decision under appeal, the Examining Division argued essentially as follows:

Claim 8 concerned an electrically-programmable, low-impedance antifuse element (36) with a first electrode on an insulating layer covering the substrate of an integrated circuit; the feature that the arsenic concentration of such a first electrode had an arsenic pile up doping profile, indicating an increased concentration at its surface, had not been disclosed originally as a general teaching.

The antifuse element of submitted claim 1 was distinguished over that known from D1 in that

- the arsenic concentration of the first electrode was not as high as 1×10^{22} atoms/cm^3;
- the doping profile thereof did not exhibit arsenic pile-up; and
- the second electrode did not consist of an arsenic-containing polysilicon.

The most important feature in the claimed device was the pile-up profile of the arsenic concentration, and this resulted from thermal oxidation of the substrate containing a high doping concentration of arsenic, this thermal oxidation forming a silicon oxide layer, i.e. the bottom layer of the dielectric layer covering the first electrode. However, there was also such an oxidizing step for fabricating the device in D1. This document related to the same technical field as the present invention and to the same technical problem, i.e. providing a reliable antifuse with a low programmed resistance, and it was not restricted to the reduction of the resistance of the layers.

Since arsenic pile-up would occur as much in D1 as it would in the application, the scientific explanation of the possible improved performance of the resulting anti-fuse above other, different devices, could not form the basis of an allowable claim.

Therefore, the subject-matter of claim 1 lacked an inventive step.

III. The applicant lodged an appeal on 9 March 1995 paying the appeal fee the same day, and filed the statement of the grounds of appeal on 22 May 1995. He requested *inter alia* that the appeal fee be reimbursed because of a substantial procedural violation. Oral proceedings were requested in the event that the application was to be refused.

IV. In response to a communication from the Board, the appellant (applicant) filed with a letter dated 4 January 1999 a new set of amended claims 1 to 13 with

two independent claims, i.e. claims 1 and 8.

Claim 1 reads as follows:

"1. An electrically programmable, low-impedance antifuse element (13) disposed in an integrated circuit, including:

a first electrode (12a, b) comprising a region in the substrate (10) of said integrated circuit containing arsenic at a concentration of between about 1 x 10^{19} to 1 x 10^{22} atoms/cm^3;

a dielectric layer (14) disposed over said first electrode; and

a second electrode (22a, 22b) comprising a layer of arsenic-containing polysilicon disposed over said dielectric layer, wherein said region has the heaviest concentration of arsenic at its interface with said dielectric layer (14)."

Claim 1 is distinguished from claim 1 forming the basis of the impugned decision in that,

after "1 x 10^{22} atoms/cm^3", the expression "said region having an arsenic pileup doping profile" has been deleted,

and in that, at the end of the claim, after "said dielectric layer", the expression

", wherein said region has the heaviest concentration of arsenic at its interface with said dielectric layer

(14)"

has been added.

Claim 8 reads as follows:

"8. An electrically-programmable, low-impedance antifuse element (36) disposed in an integrated circuit, including:

a first electrode (46) disposed on an insulating layer (42), said first electrode comprising a layer of arsenic-containing polysilicon;

a dielectric layer (48) disposed over said first electrode; and

a second electrode (50) comprising a layer of arsenic-containing polysilicon disposed over said dielectric layer;

wherein the heaviest arsenic concentration of said first electrode is at its interface with said dielectric layer."

Claim 8 is distinguished from claim 8 having formed the basis of the impugned decision in that,

after "said first electrode comprising a layer of arsenic-containing polysilicon", the expression ", wherein the arsenic concentration of said first electrode has an arsenic pile up doping profile" has been deleted,

and in that, the expression

"; wherein the heaviest arsenic concentration of said first electrode is at its interface with said dielectric layer"

has been added at the end of the claim.

V. The appellant requests that the decision under appeal be set aside and that a patent be granted on the following patent application documents:

Description:

Pages 1 to 3, 5, 7, 9, 12, 13, 16 and 20, of the application as filed;
Pages 4, 4a, 6, 8, 10, 11, 14, 15, 17, 19, 21, 22, 23 and 24, filed with appellant's letter dated 4 January 1999;

Claims:

Nos. 1 to 13, filed with the appellant's letter dated 4 January 1999;

Drawings:

Sheet No. 1 of the application as filed;
Sheets Nos. 2, 3 and 4, filed with the appellant's letter dated 4 January 1999.

Moreover, the appellant informed the Board that page 18 of the application as filed was to be deleted, and requested that oral proceedings be appointed before any

decision to refuse the application or to uphold the impugned decision of the Examining Division.

In addition, the appellant requested reimbursement of the appeal fee.

VI. The appellant submitted the following arguments in support of his request:

Inventive step:

D1 is the closest prior art. This document relates to the same technical field as the present invention and to the same technical problem, i.e. providing a reliable antifuse with a low programmed resistance. However, whereas D1 is concerned with the sheet resistance of the two electrodes and that it be low enough, in the present application, on the contrary, a reliable antifuse with a low resistance is produced by using a high concentration of arsenic near the electrode-dielectric interface which provides conductive material for the link or filament once the antifuse is blown. This is not suggested by D1 and also does not take place when carrying out the process described in D1. Therefore, the subject-matter of claim 1 involves an inventive step, and this also applies to claim 8, which concerns a device of the same type, but with the first electrode located on an insulating layer over the substrate of an integrated circuit.

Procedural violation:

Concerning the examination proceedings, it is to be

noted that the decision under appeal, e.g. at point 1.4 and 4.1 of the reasons, includes several technical assertions for which no justification is given and which had not previously been raised; accordingly, the applicant had no opportunity to comment on these alleged facts or provide counter evidence; this is contrary to the right to be heard according to Article 113(1) EPC and is thus a serious procedural violation. This applies in particular to the assertion in the decision under appeal that arsenic pile-up does not occur in polysilicon, which is incorrect. Therefore, reimbursement of the appeal fee is justified.

Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of the amendments*

In the application as amended, original Figure 3 has been deleted, and any suggestions that the highest concentration of arsenic at the interface with the dielectric layer is an optional feature have been corrected.

The expression in claim 8 containing the terms "arsenic pile up", which had been objected to in the impugned decision, has been replaced, as suggested in the communication of the Board, by the expression "wherein the heaviest arsenic concentration of said first electrode is at its interface with the dielectric layer", which has a basis on page 6, penultimate paragraph and the sentence bridging pages 7 and 8, of

the application as filed.

Therefore, the Board is satisfied that the present application meets the requirement of Article 123(2) EPC, that a European patent application may not be amended in such a way that it contains subject-matter which extends beyond the content of the application as filed.

3. *Inventive step*

3.1 Document D1 is the closest prior art and discloses:

an electrically programmable, low-impedance antifuse element disposed in an integrated circuit (see in particular the embodiment illustrated by Figure 1), said element including:

- a first electrode (12) comprising a region (12) in the substrate (10) of said integrated circuit containing arsenic at a concentration of between about 1×10^{19} to 1×10^{21} atoms/cm^3;

- a dielectric layer (14, 16, 18) disposed over said first electrode (12); and

- a second electrode (20) comprising a layer of heavily N-type doped polysilicon disposed over said dielectric layer.

However, contrary to the element of present claim 1, in the known element, in particular,

- the region (12) of the substrate comprised in the

first electrode has not the heaviest concentration of arsenic at its interface with said dielectric layer; and

- the second electrode does not consist of an arsenic-containing polysilicon.

3.2 Document D1 relates to the same technical field as the present invention and to the same technical problem, i.e. providing a reliable antifuse with a low programmed resistance; the approach to the solution of that problem is, however, fundamentally different in D1. D1 is concerned with providing relatively low sheet resistance of the two electrodes(see for instance column 6, line 55 to column 7, line 2; column 7, lines 35 to 52 and column 8, lines 8 to 15).

In D1 (see column 10, lines 56 to 58), the dielectric layer comprises an oxide layer which can be thermally grown or deposited. However, it cannot be derived from the document that thermally growing 20 or 50 Angstroms of silicon oxide would cause any profile of the arsenic in said region such that the heaviest concentration of arsenic is at its interface with said dielectric layer, irrespective of the temperature at which it is carried out.

The essential teaching of D1 is to reduce the sheet resistance of the electrodes, so that the skilled person would not be prompted to adapt the process of oxide growing in such a way that the heaviest concentration of arsenic is at the interface of the electrode with the dielectric layer. Such an information is in any case not included in D1.

In the present application (see page 5, line 8 to page 9, line 19), on the contrary, a reliable antifuse with a low resistance is produced by using a high concentration of arsenic near the electrode-dielectric interface which provides conductive material for the link or filament once the antifuse is blown.

3.3 The further prior art documents are less relevant and not directly adapted for a combination with D1, so that, having regard to the state of the art, the subject-matter of present claim 1 is not obvious to a person skilled in the art. In the Board's judgment, therefore, claim 1 involves an inventive step within the meaning of Article 56 EPC.

3.4 The above reasoning applies to claim 8, which concerns a device wherein the heaviest concentration of arsenic in the first electrode is at its interface with a dielectric, as in claim 1.

The same also applies to the dependent claims 2 to 7 and 9 to 13, which concern particular forms of the devices defined by the main claims 1 and 8, respectively.

4. Therefore, the subject-matter of the application in suit is patentable in the sense of Article 52(1) EPC and, consequently, a patent can be granted (Article 97(2) EPC).

5. *Reimbursement of the appeal fee*

The term "grounds" in Article 113(1) EPC is to be interpreted as referring to the essential reasoning,

both legal and factual, which leads to the refusal of an application (cf. decision D 951/92, OJ EPO 1996, 53). Thus, before a decision refusing an application for non-compliance with a requirement of the EPC is issued, the applicant must be informed by the EPO of the essential legal and factual reasons on which the finding of non-compliance is based, so that he knows in advance of the decision both that the application may be refused and why it may be refused, and so that he may have a proper opportunity to comment upon such reasons and/or to propose amendments so as to avoid refusal of the application (cf. T 951/92).

In its communication dated 3 September 1998, the Board informed the appellant of the reasons why, in its judgement, the decision under appeal was in keeping with the teaching of decision T 951/92. The Board is indeed satisfied that the essential legal and factual reasons for the findings that the application in suit did not comply with the requirements of Articles 123(2) and 56 EPC were (i) set out under points 1.1 to 1.3 and point 2 of the decision under appeal, respectively, and (ii) discussed at the oral proceedings before the Examining Division and/or communicated to the appellant in the written proceedings before that department.

Consequently, the appellant's submission that a substantial procedural violation occurred during the proceedings before the Examining Division cannot be accepted by the Board. From this, it follows that the requirements of Rule 67 EPC are not met in the present case; the request for reimbursement of the appeal fee has therefore to be refused.

8. *Request for oral proceedings*

With letter dated 4 January 1999, the appellant requested that oral proceedings be appointed before any decision to refuse the application or to uphold the decision under appeal be taken.

As the application is not refused, the oral proceedings are not needed (Art. 113(1) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with the following documents:

Description:

Pages 1 to 3, 5, 7, 9, 12, 13, 16 and 20, of the application;
Pages 4, 4a, 6, 8, 10, 11, 14, 15, 17, 19, 21, 22, 23 and 24, filed with appellant's letter dated 4 January 1999;

Claims:

Nos. 1 to 13, filed with appellant's letter dated 4 January 1999;

Drawings:

Sheet No. 1 of the application;
Sheets Nos. 2, 3 and 4, filed with appellant's letter dated 4 January 1999.

3. The request for the reimbursement of the appeal fee is rejected.

The Registrar: The Chairman:

D. Spigarelli R. Shukla