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D E C I S I O N
of 11 May 2000

Case Number: T 0382/95 - 3.4.3

Application Number: 90105245.6

Publication Number: 0388891

IPC: H01L 27/112

Language of the proceedings: EN

Title of invention:
Semiconductor device

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56, 123

Keyword:
"Amendment admissible (yes) implicit disclosure of a feature in the application as filed"
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0382/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3-4-3
of 11 May 2000

Appellant: Kabushiki Kaisha Toshiba
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 18 January 1995 refusing European patent application No. 90 105 245.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
M. J. Vogel

Summary of Facts and Submissions

I. The appeal lies against the decision of the Examining Division, dated 18 January 1995, refusing European patent application No. 90 105 245.6. The application was refused on the grounds that independent claims 1 and 12 of the main request did not meet the requirements of Articles 52(1), 54(1) and (2) EPC, and that an independent claim combining the subject-matter of claims 12 and 13 of the main request, submitted as an auxiliary request, did not meet the requirements of Articles 52(1) and 56 EPC.

The following prior art documents were considered in the decision under appeal:

D1: IBM Technical Disclosure Bulletin, volume 29, No. 8, January 1987, pages 3387 to 3388:

D2: Patent Abstracts of Japan, volume 12, No. 146 (E-605)[2993], 6 May 1988; and JP-A-62263653;

D3: IBM Technical Disclosure Bulletin, volume 21, No. 7, December 1978, pages 2801 to 2802; and

D4: "Microelectronic-Technologie", K. Schade, editor, Verlag Technik, Berlin 1991, pages 440 to 443.

The notice of appeal was filed on 15 March 1995 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 3 May 1995.

II. At the oral proceedings the applicant submitted the following request replacing the previous main request

and two auxiliary requests:

Claims: 1 to 12

Description: page 1 to 3, 3a, 4 to 8

Drawings: 1/3 to 3/3

Claim 1 of the request reads as follows:

"A programmed semiconductor device, comprising:

a semiconductor body (10);

semiconductor elements (MC) in said semiconductor body (10);

a wiring pattern (PT) on said semiconductor body (10) for wiring said semiconductor elements (MC), the wiring pattern (PT) including discontinuous portions (DL, BL), each discontinuous portion having a first section (DL) and a second section (BL); and

an insulating layer (15) covering said wiring pattern (PT) and defining a plurality of openings (OP), each of the openings exposing a selected discontinuous portion (DL, BL) having the first section (DL) electrically isolated from the second section (BL); and

conductive material filled in said openings to selectively connect said first and second sections;

characterised in that

said insulating layer is the final passivation layer

(15) formed on the top of the semiconductor device."

Independent claim 11 relating to a process reads as follows:

"11. A process for producing a programmed semiconductor device, comprising the steps of:

forming semiconductor elements (MC) on a semiconductor body (10);

forming first portions (DL) of a wiring pattern (PT) on the semiconductor body (10), for wiring the semiconductor elements (MC); and

Forming a plurality of discontinuous portions (BL) of the wiring pattern (PT) of an insulating layer (20) of the semiconductor body (10); and

covering the wiring pattern (PT) with the final passivation layer (15) on the top of the semiconductor device;

forming openings (OP) in said passivation layer (15) to selectively expose the ends of discontinuous portions (DL, BL) of said wiring pattern (PT), and

depositing conductive material (16) on the ends of the exposed discontinuous portions (DL, BL) via said openings (OP) to connect them together."

Claims 2 to 10 and 12 are dependent claims.

III. The applicant submitted in support of his request that the inventions claimed in product claim 1 and the

corresponding process claim 11 were new and not obvious over the cited prior art documents.

Concerning novelty, the applicant argued that

(i) claim 1 related to a programmed semiconductor device, that is to say a semiconductor device for which the programming operations have been completed; and

(ii) that the insulating layer covering the wiring pattern was the final passivation layer of the semiconductor device.

In the device known from document D1, on the other hand, customisation is performed by the formation of a second metallisation and interconnection vias on a layer which, although being an insulating layer overlying the first metallisation, is not the final passivation layer of the device. Following deposition of the second metallisation, deposition of a final passivation layer is required to protect the device against environmental influences. The appellant further submitted that the insulating layer above the first metallisation layer, which is implicit in the structure disclosed in document D1, cannot be the final passivation layer. Any insulating layer that serves as a passivation layer to protect the device during storage would itself during storage be contaminated by environmental influences, such as by absorption of water. It would therefore need to be at least partly removed before the second metallisation layer could be deposited.

Concerning the inventive step of the claimed invention,

the appellant argued that the invention as claimed solved the problem of how to reduce the turnaround time for semiconductor devices of this kind that is to say, the time between receipt of an order and shipping of devices programmed in accordance with the received order. The invention as claimed in claim 1 required fewer processing steps than prior are devices, and was based on the appreciation that the device could be programmed after the final passivation layer protecting the device had been formed. In contrast, the device known from document D1 required further processing including the second metallisation and the subsequent formation of the final passivation layer. The device known from D1 was accordingly a more complex structure, programming of which was more time consuming and hence more expensive. Neither document D1 nor any of the other cited documents gave any hint that a device structure was possible which was programmed after the formation of the final passivation layer.

The argument submitted in respect of the novelty and inventive step of the claimed device applied, *mutatis mutandis*, to the method claimed in independent claim 11.

Reasons for the Decision

1. *Amendments*

Claim 1 of the appellant's request differs from claim 1 as originally filed in that

(i) the claim is to a programmed semiconductor device,

(ii) the preamble of the claim lists the features common to the invention and the nearest prior art in document D1, and

(iii) the insulating layer is defined to be the final passivation layer formed on top of the semiconductor device.

In the application as filed, the manufacture of the claimed device is described as proceeding in the following manner. After formation of semiconductor elements such as MOS transistors (page 4, lines 23 to 26) or a gate array (page 8, lines 7 to 8), a wiring pattern is formed for wiring the semiconductor elements (page 3, lines 8 to 10, page 5 lines 19 to 30, page 8 lines 13 to 15). The wiring pattern is covered by an insulating layer (page 3, lines 10 to 11) which is also referred to as a passivation layer (page 6, lines 1 to 6 and page 8, lines 13 to 16).

The device is subsequently customised on receipt of an order by forming openings in the passivation layer to expose portions of conductors to be connected and then filling the openings with a metal conductor to establish the electrical connection. The portions of the conductors to be connected may, for example, be end portions of drain electrodes DL and bit lines BL (page 6, lines 23 to 24; page 8, lines 16 to 17).

In every case the wiring pattern and the passivation layer are formed before any order for a customised device is received (page 3, lines 16 to 19, page 6, lines 7 to 8, page 8, lines 13 to 15), and customisation is accomplished thereafter by forming the

openings at selected locations and filling them with a metal conductor. It is not necessary to perform the steps of depositing a conductive layer, patterning the layer to form the second layers of wiring, and forming an insulating layer which covers and protects the patterned conductive layer (page 3, lines 21 to 25).

It follows from the foregoing that, in order to complete the manufacture of a programmed device, no further protective layers are formed or need to be formed after the deposition of the passivating layer 15. The passivation layer thus constitutes the passivation layer which provides the final passivation of the device. Although not explicitly referred to as such in the application, the Board is satisfied that the term "final passivation layer" as applied to the aforementioned passivation layer is unambiguous, and implicit in the application as a whole.

The corresponding amendment which introduces the term final passivation layer into claim 1 does not include any matter going beyond the content of the application as filed and therefore complies with the provisions of Article 123(2) EPC.

In further amendments to the claim, claim 2 has been cancelled and the claims 3 to 13 renumbered as claims 2 to 12. Also, renumbered claims 2, 3 and 4 have been amended to make their terminology consistent with claim 1 regarding the sections (DL) and the passivating layer (15). None of these amendments introduces any new subject-matter and together with minor additional amendments to claims 10 and 12 are therefore allowable under Article 123(2) EPC.

The amendments made to the description merely serve to adapt the description to the amended claims within the provision of Article 123(2) EPC.

Independent claim 11 relating to a process for producing programmed semiconductor device in which the insulating layer is the final passivation layer, is for the same reasons considered to comply with the requirements of Article 123(2) EPC.

2. *Novelty*

Document D1 is the nearest prior art. The document discloses a programmable semiconductor device in which the programming is performed by means of a second metallisation layer i.e. conductors (6), interconnection vias (7) and conductor pads (8) (cf. page 3388, last but one paragraph).

In the terminology of claim 1 of the application in suit, document D1 discloses a programmed semiconductor device comprising:

a semiconductor body (wafer 1);

semiconductor elements (transistor structures 2) in said semiconductor body;

a wiring pattern (first metallisation conductors 3) on a semiconductor body for wiring said semiconductor elements, the wiring pattern including discontinuous portions (interruptions 5), each discontinuous portion having a first section and a second section; and

each of the openings exposing a selected discontinuous portion having the first section electrically isolated from the second section - see page 3388, penultimate paragraph;

each of the openings being filled with conductive material (conductor pads 8) to selectively connect said first and second sections.

Moreover, document D1 clearly refers to the use of vias (7) to provide connections between the conductors of the first and second metallisations and to bridge interruptions 5 of the conductors of the first metallisation (page 3388 last but one paragraph). The use of an intermediate insulating layer in which the vias are formed, covering the first metallisation is thus clearly implied in the device of document D1. This was not disputed by the appellant.

However, in the Board's view, it is evident that the insulating layer in which the openings are formed for selectively connecting the discontinuous portions of the wiring pattern is not the final passivation layer as in the invention as claimed in claim 1. In contrast to the claimed structure, the structure described in document D1 is an intermediate structure and requires a final protective layer, i.e. a passivation layer on the second metallisation, to complete the device.

The Board therefore concludes that the programmed semiconductor device claimed in claim 1 is novel.

The same considerations apply concerning the novelty of the independent process claim 11. The claim is to a process for producing a programmed semiconductor device

in which the wiring pattern is covered with the final passivation layer, the programming steps consisting of selectively forming openings in the passivation layer and depositing conductive material in these openings, thereby to connect the ends of the discontinuous portions of the wiring pattern exposed by those openings. The connection achieved by metal filling the previously formed openings in the passivation layer, thus constitutes, in effect, a conductive plug. The Board accepts the applicant's submission that, in contrast to what is taught by document D1, no further protective layer or layers are required and that the method claimed in claim 11 is therefore novel.

3. *Inventive step*

It is known from document D1 that gaps formed in the conductors of the first metallisation may be linked by conductive pads as part of the second metallisation process (page 3388, lines 31 to 33, and references 5 and 8 in Figures 1 and 2, respectively).

In a programmed device as claimed in claim 1, holes formed in the final passivation layer of the device, at selected positions above gaps in the underlying wiring pattern, are filled with conductive material that bridges the gaps and so provides electrical continuity. Formation of a further passivation layer is not required, making for a structure which is less complex and quicker to customise than the structure taught in document D1. In the Board's view, neither document D1 nor any of the other cited documents provides any assistance in arriving at a device programmed by holes formed in the final passivation layer and filled with metal. Indeed, as was argued by the applicant and

accepted by the Board, the skilled person would have been inclined to avoid opening the passivation layer because doing so could adversely affect the integrity of the semiconductor device.

The foregoing discussion applies equally to the process claim 11 which claims a process for producing a programmed semiconductor device in which the programming of the device is performed, after deposition of the final passivation layer, by forming openings in that passivation layer to selectively expose the ends of discontinuous portions of the wiring pattern and depositing conductive material via said openings to connect. Again, neither document D1 nor any of the other cited documents provide any assistance towards arriving at this method of programming a device which is less complex, quicker and therefore cheaper than the methods used to make and program a device, as in the prior art document D1.

For the foregoing reasons in the Board's judgement, the invention as claimed in claims 1 and 11 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant the patent with the following documents filed during the oral proceedings:

Claims: 1 to 12

Description: pages 1 to 3, 3a, 4 to 8

Drawings: sheets 1/3 to 3/3

The Registrar: The Chairman:

D. Spigarelli R. Shukla