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D E C I S I O N
of 12 November 1999

Case Number: T 0284/95 - 3.4.3

Application Number: 86201651.6

Publication Number: 0216435

IPC: H01L 21/76

Language of the proceedings: EN

Title of invention:
Bipolar integrated circuit having an improved isolation and substrate connection, and method of preparing the same

Patentee:
Advanced Micro Devices, Inc.

Opponent:
Koninklijke Philips Electronics N.V.

Headword:
Bipolar integrated circuit/ADVANCED MICRO DEVICES

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0284/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 12 November 1999

Appellant: (Proprietor of the patent)
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Decision under appeal: **Decision of the Opposition Division of the European Patent Office posted 27 January 1995 revoking European patent No. 0 216 435 pursuant to Article 102(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
A. C. G. Lindqvist

Summary of Facts and Submissions

I. The appellant is the proprietor of European patent No. 0 216 435 which had been granted on the basis of European patent application No. 86 201 651.6.

II. The respondent filed an opposition against the European patent citing *inter alia* documents P1: US-A-3 992 232 and P5: US-A-4 320 411 and arguing that the subject-matter of the claims did not involve an inventive step.

III. The patent, in amended form, was revoked for lack of inventive step by the decision of the opposition division dated 27 January 1995.

Claim 1 forming the basis of said decision had the following text:

"1. A structure comprising a semiconductor substrate (102) having a first conductivity type, an epitaxial layer (104) formed on said substrate (102) having a second conductivity type opposite said first conductivity type, a transistor (100) having a base (100b), an emitter (100e) and a collector (100c) formed in said epitaxial layer (104), a nonconductive region (110) laterally surrounding said transistor (100), said nonconductive region (110) extending from the surface of said epitaxial layer (104) to said substrate (102), a conductive region (112) of said first conductivity type laterally surrounding said nonconductive region (110), said conductive region (112) extending from the surface of said epitaxial layer (104) to said substrate (102), said conductive region (112) comprising monocrystalline semiconductor material, and a buried

layer (106) formed in said substrate (102), said buried layer (106) being laterally surrounded by said nonconductive region (110), characterized in that said buried layer (106) is laterally spaced apart from said nonconductive region (110)."

The decision of the opposition division was reasoned in substance as follows:

Closest prior art is document P1, which shows in Figure 1f all the features of the first part of claim 1.

However, in document P1, the buried layer (2) is not laterally spaced apart from the surrounding non-conductive region (5), but it is in contact therewith.

The characterising feature of claim 1 that the buried layer is laterally spaced apart from the surrounding non-conductive region enables, according to the patent, the provision of a device with a surface area which is small as compared to a device wherein the buried layer is in contact with the surrounding non-conductive region.

However, the desire to increase the scale of integration is almost universal in the present technical field of integrated circuits and thus the object of the invention of the opposed patent, in itself, does not contribute to an inventive step. Moreover, the specific link between the reduced surface area of a device and the spacing of a buried region from the surrounding isolation region is recognized in document P5 (see in particular column 1, lines 27 to

41; column 3, lines 25 to 47 and column 4, lines 30 to 35) so that the skilled person can appreciate the savings in space made possible by providing a device region isolated from neighbouring device regions by a surrounding non-conductive region from which the buried layer is spaced, and act accordingly. Therefore, it was obvious to combine both documents.

In this respect, the proprietor had pointed out that Figures 1A to 1C of document P5 illustrate the disadvantages of buried regions spaced from surrounding non-conductive regions whereby, in the parasitic transistor formed therein and comprising in particular the surrounded epitaxial region and the substrate, the amplification was not being reduced enough and allowed leakage current. However, this argument was not considered as convincing because this disadvantage was also known from document P1 wherein the problem was solved in particular by providing the improved substrate grounding by using the surrounding conductive region contacting it and because it was known from column 3, lines 52 to 55 of said document that the formation of a parasitic transistor was also prevented in such a structure even without a buried layer.

For this reason, the skilled person would not be discouraged from combining a buried layer of reduced extension, as the spaced buried layer of document P5, with the isolation structure of document P1 in order to provide a device with a reduced space requirement that also has adequate protection against parasitic transistor action. Therefore, the subject-matter of claim 1 lacked an inventive step.

IV. The patent proprietor lodged an appeal against this decision on 24 March 1995 paying the appeal fee the same day and, in his statement setting out the grounds of appeal received on 29 May 1995, requested *inter alia* oral proceedings auxiliarily.

In the statement of grounds of appeal, the appellant (patent proprietor) requested that the decision under appeal be set aside and that the patent be maintained in amended form with the same text as that having formed the basis for the decision under appeal, except for a new replacement description page 3 filed with the statement of the grounds of appeal. The appellant argued in substance as follows in support of his request:

The buried region (2) of document P1 contacts the non-conductive region (5) which laterally surrounds it and, thus, said buried layer (2) must be sufficiently spaced apart from the conductive region (3') of said first conductivity type laterally surrounding said non-conductive region (5). On the other hand, in the structure in dispute, since the buried region (106) is spaced apart from the non-conductive region (110) which laterally surrounds it, it is also spaced farther apart from said conductive region (112) and, thus, said non-conductive region (110) can be made smaller than the isolating structure (5) in document P1, thereby resulting in a construction using a surface area smaller than that in document P1.

Document P5 teaches that size reduction results from decreasing the depth of the dielectric isolation, and not that spacing the buried layer away from the

isolation reduces size. Thus, in short, spacing between buried layer (42) and dielectric surrounding region (43) is irrelevant to the size reduction in document P5.

Moreover, an important feature of the structure of document P5, which thus should be taken into account when combining with document P1, is a supplementary dielectric region (44) extending through the epitaxial layer from the upper surface thereof and penetrating into the buried layer, said supplementary dielectric region surrounding the most important part of the transistor and having the function of a leakage current blocking region. However, such a supplementary dielectric region (44) also adds to the space to be utilized in the structure in addition to the surrounding non-conducting region (43), so that it goes against the purpose of saving space in the structure and thus making it smaller.

Indeed, in the structure including this additional leakage current blocking region (44) of document P5, the arrangement of base, emitter and collector in the transistor described in document P1 differs from the arrangement in the transistor described in document P5.

Therefore, it is only by hindsight that the skilled person could combine the teachings of document P1 and document P5 and thus arrive in an obvious way at the claimed structure, which therefore involves an inventive step.

V. The respondent requested that the patent should be revoked and the appeal should be dismissed. He also

requested oral proceedings auxiliarily.

VI. In response to a letter from the Board informing the parties that the Board intended to appoint oral proceedings requested by the parties, the appellant informed the Board by a telefax dated 9 August 1999 that he would not attend oral proceedings which were to be scheduled for 16 November 1999.

The appellant was informed by a telefax dated 12 August 1999 from the Board that unless the Board heard from the appellant to the contrary within a week, the appellant's statement in his telefax dated 9 August 1999 would be regarded as the withdrawal of his request for oral proceedings. The appellant having failed to respond within the set time limit, there was no request for the oral proceedings by the appellant, and he was informed accordingly in a letter dated 1 September 1999.

Reasons for the Decision

1. The appeal is admissible.

2. The only issue in dispute in the present appeal is that of inventive step.

2.1 It has not been disputed by the appellant that the structure known from document P1 (see in particular Figure 1f) corresponds to the first part of claim 1.

The known structure comprises a semiconductor substrate

(1) having a first conductivity type (P), an epitaxial layer (4) formed on said substrate (1) having a second conductivity type (N) opposite said first conductivity type, a transistor having a base (8), an emitter (9) and a collector (4) formed in said epitaxial layer (4); the structure further comprises, a non-conductive region (5) laterally surrounding said transistor, said non-conductive region (5) extending from the surface of said epitaxial layer (4) to said substrate (1), a conductive region (3') of said first conductivity type (P) laterally surrounding said non-conductive region (5), said conductive region (3') extending from the surface of said epitaxial layer (4) to said substrate (1), said conductive region (3') comprising monocrystalline semiconductor material, and a buried layer (2) formed in said substrate (1), said buried layer (2) being laterally surrounded by said non-conductive region (5).

However, contrary to the structure of claim 1 in dispute and of Figure 1 of the patent in suit wherein the buried layer (106) is laterally spaced apart from the surrounding non-conductive region (110), the buried layer (2) of the known structure is shown as being in contact with the surrounding non-conductive region (5).

2.2 It has also not been disputed by the appellant that the feature distinguishing claim 1 of the patent in suit from document P1 is known from document P5 (see in particular Figures 1A to 1C, 4A to 4C, 5A and 5B and the corresponding text) wherein there are shown structures with the buried layer (7, 17, 27; 42) in a device such as a transistor being laterally spaced apart from the surrounding non-conductive region

(8, 18, 28; 43).

However, the structure of document P5 does not comprise a conductive region of the same conductivity type as the substrate extending from the surface of the epitaxial layer to the substrate and surrounding the non-conducting region and the device therein.

2.3 The appellant has firstly argued as follows with respect to the feature distinguishing claim 1 in dispute from document P1:

Since the buried region (2) of document P1 contacts the non-conductive region (5) which laterally surrounds it, said buried layer (2) must be sufficiently spaced apart from the conductive region (3') of said first conductivity type laterally surrounding said non-conductive region (5).

In the structure in dispute, on the other hand, since the buried region (106) is spaced apart from the non-conductive region (110) which laterally surrounds it, it is also spaced farther apart from said conductive region (112) and, thus, said non-conductive region (110) can be made smaller than the isolating structure (5) in document P1, thereby resulting in a construction using a surface area smaller than that in document P1.

However, this argument of the appellant is not found convincing for the following reasons:

As credibly argued in the decision under appeal and also in the observations of the respondent, a person skilled in the art of integrated circuit devices will

always strive towards a more compact structure. Moreover, the person skilled in the art also knows from document P5 (see column 1, lines 27 to 41; column 3, lines 25 to 47; Figures 1A and 1B) that a buried layer which is not spaced apart from the non-conductive region surrounding it occupies more space than a buried layer which is spaced apart from the non-conducting region because, as shown and explained in document P5 (see column 4, lines 30 to 35; see also Figure 4A), in the latter case, the non-conductive region then must not extend through the epitaxial layer and the buried layer into the substrate, i.e. must not extend more deeply and thus necessarily have a larger width.

Indeed, the appellant has also submitted in this respect that the cited passage of document P5 teaches that size reduction results from decreasing the depth of the dielectric isolation, and not that spacing the buried layer away from the isolation reduces size, i.e., in short, that spacing between buried layer (42) and dielectric (43) is irrelevant to the size reduction in document P5.

This other argument cannot convince either since it is directly and unambiguously derivable from the cited text locations and the Figures of document P5 that it is because there is no need for the isolation region to extend through the buried layer between the substrate and the epitaxial layer that its depth and consequently its width can be reduced.

2.4 Moreover, the appellant has submitted that an important feature of the structure of document P5 is a supplementary dielectric region (44) extending through

the epitaxial layer from the upper surface thereof and penetrating into the buried layer, said supplementary dielectric region surrounding the most important part of the transistor and having the function of a leakage current blocking region. However, this argument cannot convince either since said supplementary leakage current blocking region (44) of dielectric material is not shown in the structure of Figures 1A and 1B of document P5, i.e., advantages arising because of the buried layer being spaced apart from the surrounding non-conducting region are also derivable with respect to said Figures 1A and 1B.

Indeed, as also argued by the appellant with respect to this additional leakage current blocking region (44) of dielectric material of document P5, the arrangement of base, emitter and collector in the transistor described in document P1 differs from the arrangement in the transistor described in document P5. However, also this argument cannot convince the Board because, as already set forth in the preceding paragraph, this additional leakage current blocking region (44) of dielectric material is not to be found in Figures 1A and 1B of document P5 which are relevant in the present assessment of the inventive step of claim 1 in dispute and, moreover, claim 1 in dispute does not specify the arrangement of the regions in the transistor and especially of the emitter, basis and collector thereof. Thus, in any case, the appellant's argument in this respect that combining structures of different transistors could be done only by hindsight cannot convince the Board.

It is also to be noted that the further advantage of

simplifying the manufacturing process pointed out by the appellant is not considered as relevant at least with respect to claim 1 in dispute, which does not concern a process.

2.5 For the foregoing reasons, in the Board's judgment, the subject-matter of claim 1 of the appellant's request is obvious to a person skilled in the art and, consequently, it lacks an inventive step in the sense of Article 56 EPC. Consequently, the claim is not patentable in the sense of Article 52(1) EPC.

2.6 Therefore, the European patent as amended by the proprietor (appellant) does not satisfy the requirements of the Convention, so that it cannot be maintained in said amended form (Article 102(3) EPC).

3. The appellant having withdrawn his request for oral proceedings (see item VI above), a decision to dismiss the appeal can be issued in compliance with Article 113(1) EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Spigarelli R. Shukla