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D E C I S I O N
of 4 May 1999

Case Number: T0036/95 - 3.4.1

Application Number: 86114320.4

Publication Number: 0222197

IPC: G07B 17/02

Language of the proceedings: EN

Title of invention:
Systems for non-volatile storage of data and postage meter
systems

Applicant/Patentee:
PITNEY BOWES INC.

Opponent:
Francotyp-Postalia Aktiengesellschaft & Co.

Headword:
Systems for non-volatile storage of data/PITNEY BOWES INC.

Relevant legal provisions:
EPC Art. 123(2)

Keyword:
"Subject-matter extending beyond the content of the application
as filed (yes; for all requests)"

Decisions cited:
-

Catchword:
-

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Boards of Appeal

Chambres de recours

Case Number: T 0036/95 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 4 May 1999

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Decision under appeal: Interlocutory decision of the Opposition Division
of the European Patent Office dated
10 November 1994 concerning maintenance of
European patent No. 0 222 197 in amended form.

Composition of the Board:

Chairman: G. Davies
Members: H. K. Wolfrum
G. Assi

Summary of Facts and Submissions

I. The appellant (opponent) lodged an appeal against the
    interlocutory decision of the opposition division,
    dispatched on 10 November 1994, maintaining European
    patent No. 0 222 197 in amended form. The notice of
    appeal was received on 11 January 1995, the prescribed
    fee being paid on the same day. The statement setting
    out the grounds of appeal was received on
    13 March 1995.

II. Opposition had been filed against the patent as a whole
    and based on Article 100(a) together with
    Articles 52(1), 54 and 56 EPC.

    Additional objections concerning lack of clarity and
    added subject-matter had been raised by the opponent
    during the opposition procedure against amended claims
    filed by the patent proprietor.

III. The appellant based the appeal on Articles 123(2) and
     123(3) EPC as well as on Articles 52(1), 54 and 56 EPC.

IV. Oral proceedings were held on 4 May 1999.

    The appellant requested that the decision under appeal
    be set aside and that the European patent be revoked.

    The respondent (proprietor of the patent) requested
    that the appeal be dismissed and the patent be
    maintained on the basis of:

    claims 1 to 3 as filed on 7.10.94 and claims 4 to 28 as
    filed on 22.9.93 with the description as maintained by
    the opposition division and the Figures as granted
    (main request);

claims 1 to 27 filed on 1.4.99 with the description to
be adapted and the Figures as granted **(first auxiliary
request)**;

claims 1 to 26 filed on 1.4.99 with the description to
be adapted and the Figures as granted **(second auxiliary
request)**; and

a set of claims omitting any unallowable claim of the
second auxiliary request **(third auxiliary request)**.

V. Independent claims 1 to 3 of the main request read
(without reference numerals) as follows:

"1. A system for the non-volatile storage of data,
comprising:
a microcomputer means;
a first non-volatile memory having data terminals
connected to said microcomputer means for having data
written into said first non-volatile memory by said
microcomputer means, said first non-volatile memory
requiring data to be applied to said first non-volatile
memory data terminals for more than a predetermined
time for data to be written into said first non-
volatile memory;
a second non-volatile memory having data terminals
connected to said microcomputer means for having said
data written into said second non-volatile memory, said
second non-volatile memory being of a type wherein a
time less than said predetermined time is a sufficient
time for data applied to said second non-volatile
memory to be written into said second non-volatile
memory; and
program store means coupled to said microcomputer means
for controlling the operation of said microcomputer
means to apply, for more than said predetermined time,
data to said first non-volatile memory data terminals
for writing data into said first non-volatile memory

and during said predetermined time to apply data to
said second non-volatile memory data terminals, so that
writing data into the second non-volatile memory is
carried out within the write cycle of the first non-
volatile memory.

2. A system for the non-volatile storage of data
comprising:
a microcomputer means;
a first non-volatile memory means having data terminals
connected to said microcomputer means for having data
written into said non-volatile memory means by said
microcomputer means, said first non-volatile memory
means requiring data to be applied to said first non-
volatile memory means data terminals for more than a
predetermined time for data to be written into said
non-volatile memory means;
an MNOS second non-volatile memory means having data
terminals connected to said microcomputer means for
having said data written into said second non-volatile
memory means, said second non-volatile memory being of
a type wherein a time less than said predetermined time
is a sufficient time for data applied to said second
non-volatile memory means to be written into said
second non-volatile memory means; and
a program store means coupled to said microcomputer
means for controlling the operation of said
microcomputer means to apply, for more than said
predetermined time, data to said first non-volatile
memory means data terminals, or read from said first
non-volatile memory means, and during said
predetermined time while accessing said first non-
volatile memory means data terminals, to apply high
value data to said second non-volatile memory means
data terminals, to protect data in said second non-
volatile memory from inadvertent overwriting.

3. A system for the non-volatile storage of data,
comprising:

a microcomputer means;

a first non-volatile memory having data terminals
connected to said microcomputer means for having data
written into said first non-volatile memory by said
microcomputer means, said first non-volatile memory
requiring data to be applied to said first non-volatile
memory data terminals for more than a predetermined
time for data to be written into said first non-
volatile memory;

a second non-volatile memory having data terminals
connected to said microcomputer means for having said
data written into said second non-volatile memory, said
second non-volatile memory being of a type wherein a
time less than said predetermined time is a sufficient
time for data applied to said second non-volatile
memory to be written into said second non-volatile
memory; and

program store means coupled to said microcomputer means
for controlling the operation of said microcomputer
means to apply, for more than said predetermined time,
data to said first non-volatile memory data terminals
for writing data into said first non-volatile memory
and during said predetermined time to apply data to
said second non-volatile memory data terminals, said
system further comprising power supply means coupled to
said microcomputer means for energizing said
microcomputer means, energy storage means electrically
coupled to said microcomputer means for energizing the
microcomputer means when energization of said
microcomputer means by said power supply means is
interrupted; and, said program store means controlling
said microcomputer means to write data only into said
first non-volatile memory means when said microcomputer

means is energized by said power supply means and to
write data into both said first and second non-volatile
memory means when said microcomputer means is energized
by said energy storage means."

Independent claims 1 to 3 of the first auxiliary
request additionally define a "redundant" non-volatile
storage of data; the first non-volatile memory to be a
"byte-oriented EEPROM of floating gate type", for data
to be written "byte-wise"; the second non-volatile
memory to be a "nibble-oriented MNOS memory", for data
to be written "nibble-wise". Two nibbles of data are
"consecutively" written to the MNOS memory in the time
that it takes for one byte of data to be written to the
EEPROM. Moreover, the alternative "or read from said
first non-volatile memory means" has been deleted from
claim 2.

The independent claims 1 and 2 of the second auxiliary
request are identical to claims 1 and 3 of the first
auxiliary request.

VI.   As regards the issue of subject-matter extending beyond
the content of the application as filed
(Article 123(2) EPC), the appellant essentially relied
on the following submissions:

Claim 1 of the main request combined features disclosed
in original claim 1 with features concerning the
simultaneous writing of the same data into both non-
volatile memories. If at all, these features could only
be derived from the description. However, there was a
contradiction between the content of original claim 1
and the description from which said amendment was
derived. Original claim 1 (as claim 1 of the main
request) required the two non-volatile memories to have
different writing times. The description, on the

contrary, disclosed memories having identical writing times for the writing of the same data. Thus, there was no basis of disclosure for the combination of features comprised in claim 1 of the main request. The same objection applied to claim 1 of the auxiliary requests.

Original claim 1 should be interpreted as referring to data to be written into both non-volatile memories. Thus, the subject-matter of claim 2 of the main and first auxiliary requests referring to "data" which were applied to data terminals but not to be stored did not find a basis of disclosure in the application as filed.

Moreover, no basis of disclosure was given for the swapping of the roles of the EEPROM and the MNOS memory as the slower and faster writing memory, respectively, with respect to original claim 4 (corresponding to claim 4 as granted), as the respondent had done in independent claims 2 and 3 of the main request and in all independent claims of all auxiliary requests.

VII. The respondent disputed the appellant's view, relying on the following arguments:

Original claim 1 (as well as claim 1 as granted) defined a system having data applied to the first non-volatile memory for at least a predetermined time, for the data to be written into this memory, and during said predetermined time data applied to the second non-volatile memory. This general definition was intended to cover the aspect that data is also written into the second non-volatile memory (as was evident from original claim 2 referring to "postage meter accounting data") as well as the aspect that data, in the most general meaning of this term, is applied to the terminals of the second memory to avoid inadvertent overwriting. In fact, claims 1 and 2 of the main

.../...

request were restricted versions of claim 1 as granted.
Details concerning the writing of data into both
memories were given in column 5, lines 6-30 of the
patent specification. The aspect of protecting one of
the memories from inadvertent overwriting while
addressing the other memory was described in column 5,
lines 37 -51. According to this disclosure, it takes
two milliseconds for data to be written into one of the
memories (an EEPROM), whereas it takes only one
millisecond to complete a write cycle for the writing
of data into the other memory (MNOS memory). Thus,
there is clear disclosure of a system having non-
volatile memories of different writing times. This
finding was confirmed when reference to the data sheets
concerning the specific types of memories mentioned in
column 9, line 44 - column 10, line 3 of the patent
specification is made. The data sheet referring to the
EAROM MNOS type "ER3400" memory disclosed a write time
of one millisecond, and the data sheet concerning the
EEPROM disclosed a type having a write time of two
milliseconds. Although the term "write cycle" was not
used in the given citations, it was clear from the
whole context of the application that its meaning was
synonymous to a writing time.

As far as the auxiliary requests were concerned, the
claims thereof were further restricted. Nothing was
broadened, deleted or shifted. Apart from that, too
much significance should not be attributed to the claim
language requiring for one of the memories a writing
time of "more than a predetermined time", since it was
in principle irrelevant whether data were applied to
the two non-volatile memories for the predetermined
time or longer.

As regards the swapping of the roles of the EEPROM and
the MNOS memory with respect to the longer or shorter
writing time compared to original claim 4, this
concerned the correction of an obvious error as it was
evident from the aforementioned citations that the
floating gate EEPROM was the memory having the longer
writing time (i.e. two milliseconds compared to one
millisecond for the MNOS memory).

Reasons for the Decision

1.   The appeal complies with Articles 106 to 108 and
        Rule 64 EPC and is therefore admissible.

2.   *Subject-matter extending beyond the content of the
        application as filed (Article 123(2) EPC)*

2.1   Main request

2.1.1   There is no literal disclosure to be found of the
        feature comprised in claim 1 of the main request "so
        that writing into the second memory is carried out
        within the write cycle of the first non-volatile
        memory".

        The disclosure provided by original claim 1 and
        corresponding dependent claims refers to a system for
        the non-volatile storage of data comprising a first
        non-volatile memory of a type requiring data to be
        applied to its data terminals for more than a
        predetermined time to be written into the memory, and a
        second non-volatile memory of a type for which a time
        less than the predetermined time is sufficient for data
        to be written into it. The original claims thus define

a system having memories of **differing writing times**.
The term "write cycle" does not occur in the original
claims.

The original description, on the other hand, discloses
a "unique system" of interleaving the writing of
identical data between an EEPROM type memory and an
MNOS type memory (cf. page 8, lines 12-31 of the
original description, corresponding to column 5,
lines 6-30 of the patent specification referred to by
both parties) in the context of a power down routine of
a postage meter system or when switching into a service
mode (cf. original page 8, lines 2-11). Data is written
into the EEPROM in units of bytes, the writing of one
byte of data taking two milliseconds. Data is written
into the MNOS type memory in units of nibbles, the
writing of one nibble of data taking one millisecond.
Due to the facts that two nibbles form a byte and that
the nibbles are consecutively written (cf. original
page 25, lines 37-38), it is evident that the writing
of the same amount of data takes **identical writing
times**. The information given on page 14, lines 2-15 of
the original description (corresponding to column 9,
line 44 - column 10, line 3 of the patent specification
as cited by the respondent) concerning specific
commercially available memories and the reference to
their respective data sheets does not give rise to a
different judgement. As far as the term "write cycle"
is used in the description (cf. original page 25,
lines 29-37 and page 27, lines 22-24), it is not
synonymous to a writing time for a byte or nibble of
data but is applied to a complex scheme of write
operations in a memory block write routine, including
for instance a waiting period for the writing into the
EEPROM during which a data header is written into the
MNOS type memory, or is used in the context of a "write
cycle endurance" of a memory.

Thus, in the present case, the original disclosure comprises separate sources of technical information which is mutually exclusive. The original claims on the one hand define a system and its operation requiring non-volatile memories of differing writing times, whereas the description explains the operation of a system having non-volatile memories of identical writing times. For a skilled reader of the application as filed, it is not apparent whether and how information relating to the operation of memories having identical writing times could be combined with generalized definitions concerning the operation of memories having differing writing times. Therefore, a combination of features as provided by claim 1 under consideration is not comprised in the content of the application as filed.

In this context, it has to be noted that a concept of "writing times" being differently defined for different memories (as relied on by the respondent in its argumentation) confuses the issue and is not suitable for a proper interpretation of a claim definition. Moreover, the argument that not too much significance should be attributed to the claim language concerning the definitions of writing times, since it was in principle irrelevant whether data were applied to the two non-volatile memories for the predetermined time or longer, cannot be accepted in view of the fact that it is exactly the exploitation of different write cycle times which, according to the contested decision, was held to form the novel and inventive concept distinguishing the patent from the prior art.

2.1.2   Claim 2 of the main request also defines a system having non-volatile memories of differing writing times and requires the memory having the shorter writing time to be an MNOS memory.

This definition is in contradiction to the content of original claim 4 defining, in combination with original claim 1, the MNOS memory as being the memory having the longer writing time. Therefore, the original claims do not provide a basis of disclosure for the subject-matter of claim 2. Nor does the description, which refers exclusively to memories having identical writing times, provide a basis of disclosure for this swapping in the writing time associated with the MNOS type memory, for the same reasons as given in paragraph 2.1.1 above.

2.1.3   Claim 3 is an amended version of original claim 3 taken in combination with original claim 1, the amendment concerning the requirement that it is the **first** non-volatile memory into which data are (exclusively) written when the microcomputer means is energized by the (regular) power supply means. In contrast thereto, original claim 3 defines the **second** non-volatile memory to be used for this purpose. Thus, as in claim 2, the writing time for the memories is swapped, and no basis of disclosure can be found for such swapping.

2.2   Auxiliary requests

The independent claims of all auxiliary requests further define the first non-volatile memory to be a byte-oriented EEPROM of the floating gate type and the second non-volatile memory to be a nibble-oriented MNOS memory. These further amendments are exclusively derived from the description. As for the claims of the main request, the claims of the auxiliary requests define the two memories to have differing writing times. Moreover, in all claims of the auxiliary requests, the writing times for the EEPROM and MNOS memory have been swapped with respect to the definition provided by the original claims.

In consequence, the claims of all auxiliary requests
define subject-matter which extends beyond the content
of the application as filed, for the same reasons as
given in paragraphs 2.1.1 to 2.1.3 above.

2.3   Therefore, none of the respondent's requests complies
with the requirements of Article 123(2) EPC so that the
requests are not allowable.

Order

For these reasons it is decided that:

The decision of the opposition division is set aside.

The patent is revoked.

The Registrar: The Chairman:

M. Beer   G. Davies