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D E C I S I O N
of 17 April 1996

Case Number: T 0683/94 - 3.5.2

Application Number: 88119034.2

Publication Number: 0316877

IPC: G11C 7/00

Language of the proceedings: EN

Title of invention:
Semiconductor memory device with improved output circuit

Applicant:
NEC CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Inventive step - yes (after amendment)

Decisions cited:
T 0248/85, T 0654/92

Catchword:
-

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Case Number: T 683/94 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 17 April 1996

Appellant: NEC CORPORATION
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 26 January 1994 refusing European patent application No. 88 119 034.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
J.-C. Saisset

Reasons for the Decision

I. The appellant contests the decision of the Examining Division refusing European patent application No. 88 119 034.2. The reason given for the refusal was that the subject-matter of claim 1 of the main request then on file did not involve an inventive step, having regard to the following prior art:

D1: US-A-4 620 298

D2: IEEE 1987 SOLID-STATE CIRCUITS CONFERENCE, DIGEST OF TECHNICAL PAPERS, February 1987, pages 264 to 265 and 420, New York, USA, OHTANI et al: "A 25 ns 1Mb CMOS SRAM".

The decision under appeal also referred to matter designated in the application as "prior art", in particular, in relation to one of the dependent claims (claim 5).

II. In a communication, the Board pointed out that this admitted "prior art" appeared not to be an appropriate starting point for the assessment of inventive step, since it appeared to be internal prior art, which was not comprised in the state of the art within the meaning of Article 54(2) EPC, citing decisions T 248/85, OJ EPO 1986, 261 (points 9.1 and 9.2) and T 654/92 of 3 May 1994. It further indicated that claim 1 appeared not to involve an inventive step having regard to D2 and common general knowledge in the art. In response to this communication the appellant filed a new independent claim, by way of a single request, and consequentially amended description.

III. Oral proceedings were held before the Board on 17 April 1996 in the course of which the appellant submitted a further amended independent claim, by way of auxiliary request, in response to the discussion.

IV. Claim 1 of the main request is now worded as follows:

"1. A semiconductor memory device comprising a first data line (38) supplied with a first data signal indicative of a data read out from a selected memory cell, a second data line (39) supplied with a second data signal indicative of an inverted one of said first data signal, an output terminal (64), and an output circuit driving said output terminal in response to said first and second data signals, characterised in that said output circuit includes a first sense amplifier circuit (33) having first and second input nodes coupled respectively to said first and second data lines and having a circuit configuration with a current mirror load for producing a first output signal through differential amplification, a second sense amplifier circuit (34) having third and fourth input nodes coupled respectively to said first and second data lines and having a circuit configuration with a current mirror load for producing a second output signal through differential amplification, said second output signal having a phase that is inverted with respect to said first output signal, a first output transistor (62) coupled between a first power line (Vdd) and said output terminal (64), a second output transistor (63) coupled between a second power line and said output terminal (64), a first driving circuit (35) activated by an output-enable signal (OE) to transfer said first output signal to said first output transistor (62), and a second driving circuit (36) activated by said output-enable signal (OE) to transfer said second output signal to said second output transistor."

Claims 2 to 5 (main request) are dependent on claim 1.

Claim 1 of the auxiliary request is worded as follows:

"1. A semiconductor memory device comprising a first data line (38) supplied with a first data signal indicative of a data read out from a selected memory cell, a second data line (39) supplied with a second data signal indicative of an inverted one of said first data signal, an output terminal (64), and an output circuit driving said output terminal in response to said first and second data signals, wherein said output circuit includes a first sense amplifier circuit (33) having first and second input nodes coupled respectively to said first and second data lines and having a circuit configuration with a current mirror load for producing a first output signal through differential amplification, a second sense amplifier circuit (34) having third and fourth input nodes coupled respectively to said first and second data lines and having a circuit configuration with a current mirror load for producing a second output signal through differential amplification, said second output signal having a phase that is inverted with respect to said first output signal, characterised by an output inverter circuit (37) comprising a first output transistor (62) of npn bipolar type coupled between a first power line (Vdd) and said output terminal (64), a second output transistor (63) of n-channel FET type coupled between a second power line and said output terminal (64), a first driving circuit (35) activated by an output-enable signal (OE) to transfer said first output signal to said first output transistor (62), and a second driving circuit (36) activated by said output-enable signal (OE) to transfer said second output signal to said second output transistor."

Claims 2 to 4 (auxiliary request) are dependent on claim 1.

V. The appellant argued essentially as follows:

Claim 1 was now delimited with respect to D2, the closest Article 54(2) prior art, rather than the internal prior art discussed in the application (Figures 1 and 2). Starting from D2, a total of five steps was involved before the person skilled in the art could arrive at the semiconductor memory device as claimed. The skilled person had to select a single-stage (single pair of complementary sense amplifiers) rather than the two-stage (two pairs of complementary sense amplifiers) arrangement of D2 (step 1) and omit the output buffer latch, not shown in the drawings of D2, but mentioned as being provided (step 2); see paragraph bridging columns 1 and 2 of page 264. Then he had to design an alternative output circuit for the device - although there was no suggestion on this subject to be found in D2 - said output circuit comprising a pair of output transistors in the configuration specified in the claim (step 3), coupled to the sense amplifier outputs by respective complementary driving circuits (step 4), said driving circuits being activated by output-enable signals (step 5).

There was no obvious objective path leading from D2 to the claimed device when such a large number of steps was involved.

Although the features of the claim corresponding to steps 3 to 5 in the above analysis were present in the "prior art" circuit of Figure 1, it was not consistent with the jurisprudence of the EPO Boards of Appeal, which stated that internal prior art was to be disregarded in assessing inventive step, to allege that certain parts of the Figure 1 circuit were part of the common general knowledge in the art.

Finally, the appellant pointed out that the European search report had rated D2 as category A ("technological background"), implying that the search examiner did not regard the subject-matter of the claims as obvious having regard to this document.

VI. The appellant requested that the decision under appeal be set aside and a patent granted on the basis of the following application documents (main request):

Claims: claim 1 filed 18 March 1996,
claims 2 to 5 filed 3 June 1994;

Description: pages 1, 6, 7, 15 filed 18 March 1996,
pages 2 to 5, 8 to 14 as originally filed;

Drawings: sheets 1 to 5 as originally filed;

or alternatively (auxiliary request) that a patent be granted on the basis of claims 1 to 4 as submitted in the oral proceedings on 17 April 1996 together with the description and drawings as specified in the main request.

Reasons for the Decision

1. The appeal is admissible.

2. *State of the art (all requests)*

The issue in this appeal is inventive step. As always, a critical preliminary step in addressing this question is the determination of the relevant "state of the art", with a view to identifying a closest prior art. Following decisions T 248/85, OJ EPO 1986, 261 (points 9.1 and 9.2) and T 654/92 of 3 May 1994 (points 4.2 and 4.3), the Board rules that the matter illustrated by and described in connection with Figures 1 and 2 of the present application is not comprised in the state of the art for the purposes of Article 56 EPC since there is no evidence before the Board that this art was made available to the public as required by Article 54(2) EPC. The effect of this ruling is explained in greater detail at point 3.3 below.

3. *Inventive step (main request)*

3.1 A semiconductor memory device comprising all the features of the prior art portion of claim 1, as delimited in the main request, is undisputedly known from D2, Figure 2. Notwithstanding the appellant's assertions to the contrary, the following features specified in claim 1 are, in the judgement of the Board, also disclosed in D2; the first and second sense amplifiers having input nodes coupled to the data lines supplied with data signals indicative of data read out from a selected memory cell, having circuit configurations with current mirror loads and producing complementary phase signal outputs correspond to the pair of amplifiers designated "Block S/A" in Figure 2 of

D2. The presence of the upstream dual amplifier stage designated "Section S/A" in the figure does not detract from this conclusion, since the claim does not specify a direct coupling of the sense amplifiers to the memory cell and the data supplied to the downstream dual amplifier stage is "indicative of a data read out from a selected memory cell" as specified in the claim. It is not disputed by the appellant that the sense amplifiers depicted in Figure 2 of D2 have circuit configurations with current mirror loads.

3.2 Starting from a semiconductor memory device as known from D2, the problem solved by the claimed device is to devise an appropriate alternative to the output buffer latch (not shown in D2, but described in the paragraph bridging the columns of page 264), which in D2 constitutes the output stage of the memory device and enables a power-down function to be implemented. No contribution to inventive step is involved in formulating this problem, given that a power-down function is a design option in the field of semiconductor circuitry, which is provided or not according to application requirements, eg low or high capacity power supply. Equally the modification specified in claim 1 (the characterising portion of the properly delimited claim), as an alternative to the D2 output buffer latch is, in effect, a pair of output transistors connected to the complementary outputs of the device terminal in a conventional push-pull arrangement and driven by complementary driving circuits in conventional fashion. Such output circuits are referred to in D1, column 1, lines 10 to 19 as being generally employed in the art and D1, Figure 4 shows an example which corresponds to the arrangement specified in claim 1 except for the fact that in the D1 circuit the driving circuits are not activated by an output-enable signal.

3.3 As regards this output-enable feature, the Board observes that activation of circuits by an "enable" control signal, to select one or more of a plurality of data transfer circuits and to define the precise time interval during which a data signal is to be transferred was notorious in the electronic art before the priority date of the present application. In this respect the Board endorses the view expressed by the Examining Division in its communications and in the decision under appeal - a view which was not contested by the appellant prior to the oral proceedings before the Board. Although it is in the nature of such a situation that the Board has to make a judgement without the benefit of independent documentary evidence on this point, the Board is nevertheless satisfied - given that its own independent expert assessment confirms the view expressed by the Examining Division having special knowledge in this field, and having regard to the fact that the output-enable feature was included in the driving circuits of the "prior art" output circuit of Figure 1 of the present application without any special comment as to its significance - that the feature concerned was part of the common general knowledge in the art of semiconductor driving circuits at the priority date of the application. This finding of the Board does not imply any contradiction with its ruling at point 2 above; an applicant's right to resile from an acknowledgement of prior art, eg as being purely internal prior art not in fact made available to the public, is not prejudiced by a finding by the Board in relation to individual features of the combination of features constituting the subject matter of the original acknowledgement. It accords with logic and experience that many such individual features will be *per se* notorious.

3.4 The appellant's argument that the semiconductor memory device as claimed in claim 1 is not obvious for the skilled person because, starting from D2, it involved five steps is not persuasive. The first alleged step of choosing to use a single stage of amplification, ie one pair of complementary amplifiers rather than two pairs as in D2, cannot be given any weight since the claim is not limited explicitly or implicitly to a single stage as explained at point 3.1 above. The second alleged step of replacing the output buffer latch by a non-latching output circuit corresponds to the formulation of the problem, which as noted at point 3.2 above, is motivated by routine considerations not making a contribution to inventive step. The remaining three alleged steps of selecting an output circuit comprising the three elements (i) push-pull output transistor pair, (ii) driving circuits and (iii) activation of the latter by an output-enable signal are, in the judgement of the Board, effectively a single solution step for the skilled person since these three elements form a cluster or sub-combination of routinely associated inter-operating components, which it would it would be obvious to employ if the circumstances did not require latching of the output.

3.5 The Board concludes therefore that, having regard to the cited prior art D2, the subject-matter of claim 1 of the main request is obvious to a person skilled in the art and is thus considered as not involving an inventive step within the meaning of Article 56 EPC.

3.6 The main request has accordingly to be rejected.

4. *Inventive step (auxiliary request)*

4.1 Claim 1 of the auxiliary request introduces a further distinction over the cited prior art in that it specifies that the pair of transistors forming the push-pull output transistor pair is constituted by an npn bipolar type and an n-channel FET type respectively, a feature which was mentioned in claim 5 of the present application as originally filed and as refused.

4.2 The European search report, which was drawn up for all claims, found nothing relevant to claim 5. In the decision under appeal, at point 6, the Examining Division found that this feature did not add anything inventive to the subject matter of claim 1 for reasons given in the communication of 16 July 1992; the relevant reason being that the output circuit referenced 14 in Figure 1 of the present application had this construction and that Figure 1 was acknowledged as "prior art".

4.3 Since the sole reason for the finding of lack of inventive step, as far as this feature of a hybrid output circuit is concerned, was the appellant's own "prior art", from the acknowledgement of which the appellant has now resiled, the Board has no objective reason to dispute the appellant's contention that it was not obvious, at the priority date of the application, for the skilled person to design the output circuit in this particular way.

4.4 The Board concludes therefore that, having regard to the cited prior art, the subject-matter of claim 1 of the auxiliary request is not obvious to a person skilled in the art and is thus considered as involving an inventive step within the meaning of Article 56 EPC.

5. In the judgement of the Board, the application documents of the auxiliary request in their present form meet the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in accordance with the appellant's auxiliary request (see paragraph VI above).

The Registrar: The Chairman:

M. Kiehl W. J. L. Wheeler